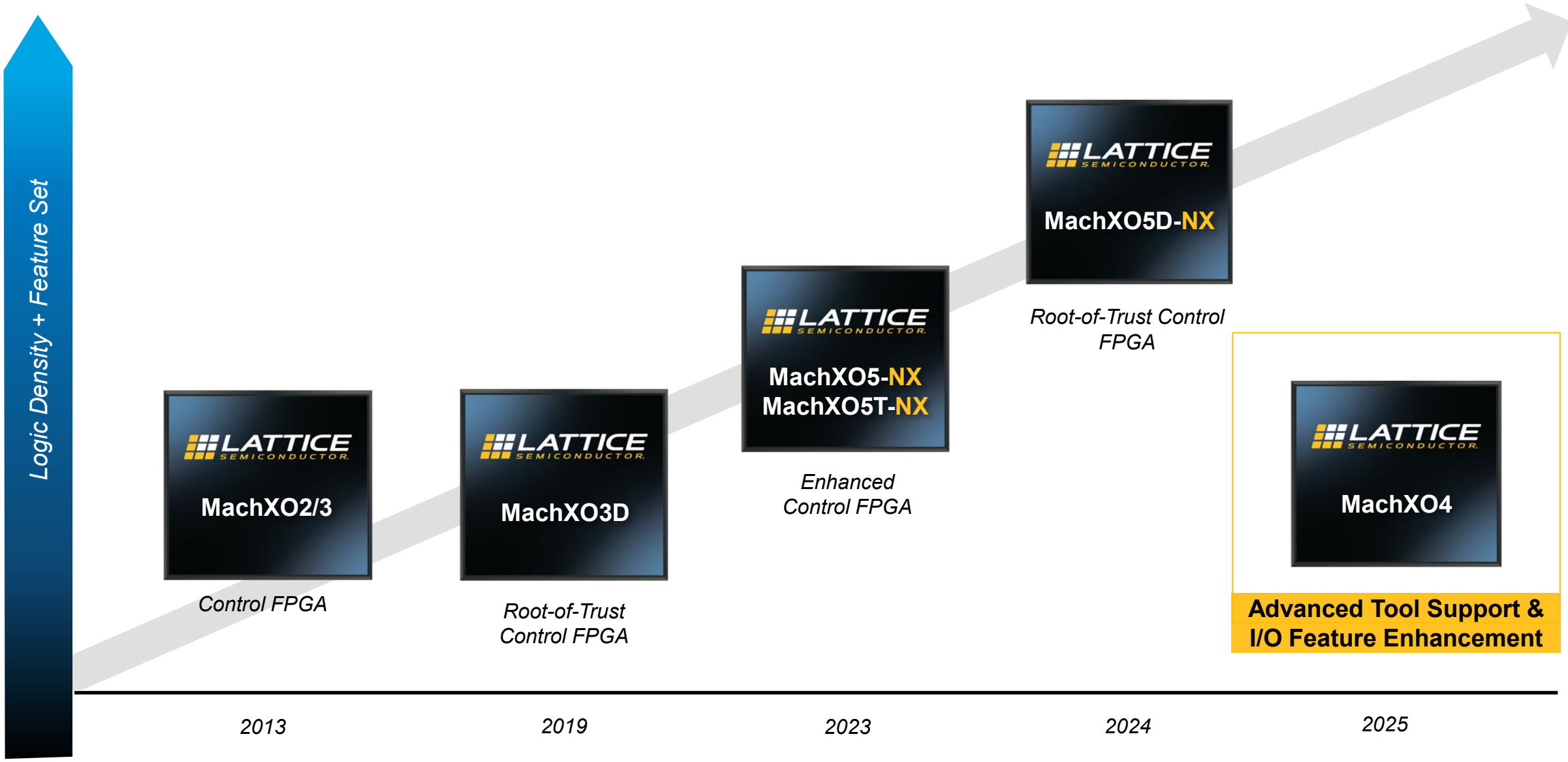
The Low Power Programmable Leader

20+ Years of Continued Innovation in the Small FPGA Market

Generations of Lattice Mach Control and Secure FPGAs

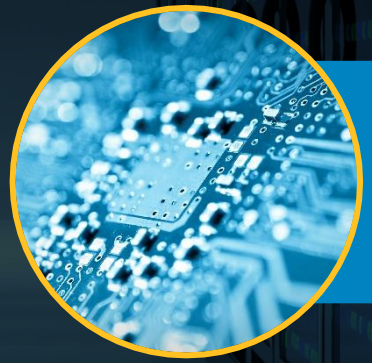


MachXO4 Differentiated Value

Highly Flexible & Robust I/O

Fast Boot Time (<5 ms) & Integrated Flash

Highest Logic Density per Package Area



Highest I/O Count per Package Area

20+ Years of Product Longevity

Low Static Power as low as 1 mW

Comparison focused on comparable products with ~10K LUTs

Instant-On (< 5ms) with Integrated Flash

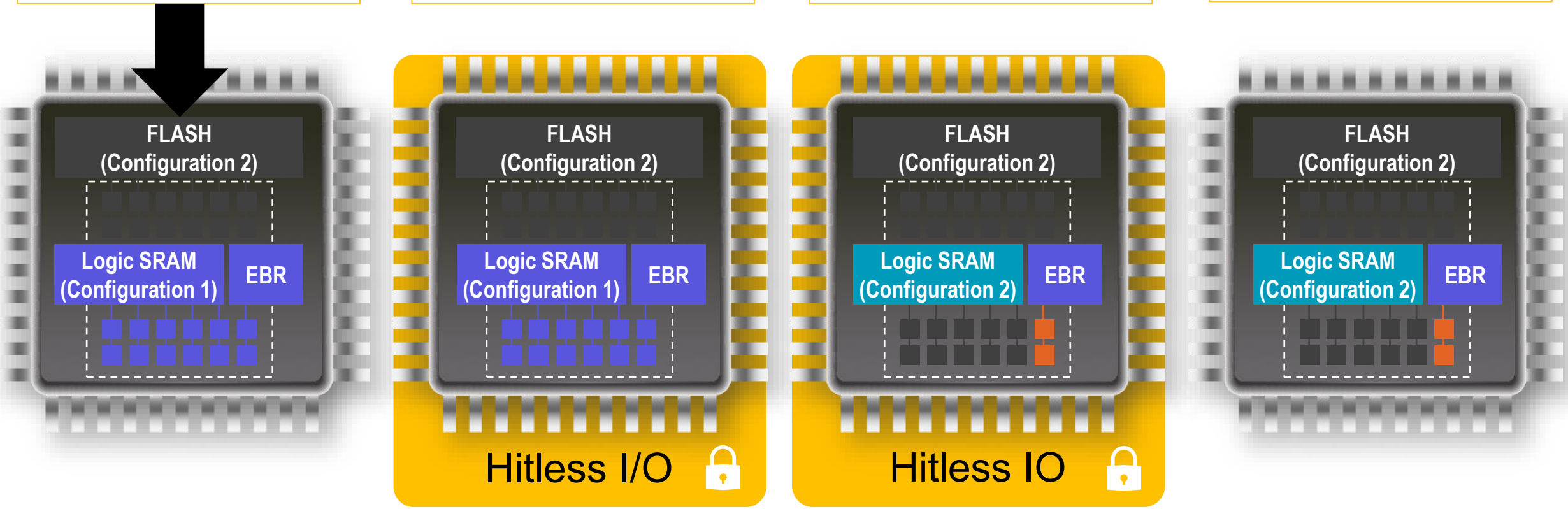
Hitless I/O & TransFR : Update FPGA w/o Interruption

STEP 1
Background Program
Load new config. to configuration memory

STEP 2
TransFR Command
Lock the I/Os in their desired state

STEP 3
Hitless I/O Active
Apply new configuration

STEP 4
New Image in SRAM
FPGA regains control of I/O



MachXO4 enables 99.999% system up time with uninterrupted field updates

Best-in Class Security

- Unique device ID
- One-time programmable mode (OTP)
- Dual-boot support
- Flash Protect Key for IP protection

Highly Flexible & Robust I/O

Highest Logic Density Per Package Area

Highest IO Count Per Package Area

Flexible I/O Solutions

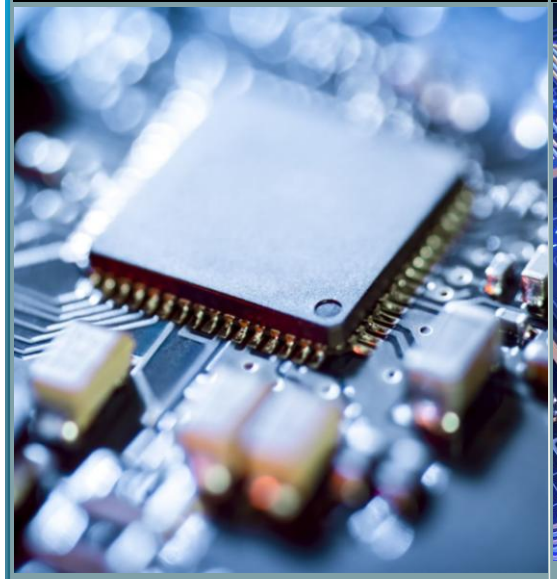
Solve I/O Challenges

- **Per-Pin Select Options**
  - Pull-up / Pull-down
  - Slew Rate
  - Drive Strength
  - Input Hysteresis
- **Hardware Flexibility**
  - Integrated Pull-down
  - Improved Hot Socketing
  - Up to 6 I/O Banks
  - Multi-Standard Support per Bank

Wide Range of I/O Standards Supported

LVTTL	LVCMOS33	LVCMOS15	LVDS
SSTL 2.5	LVCMOS25	LVCMOS12	MIPI
SSTL 1.8	LVCMOS18	LVCMOS10	

1V I/O Support



- Direct interface to modern CPUs
- Remove GTL buffers
- Input and bidirectional support

900 Mbps I/O

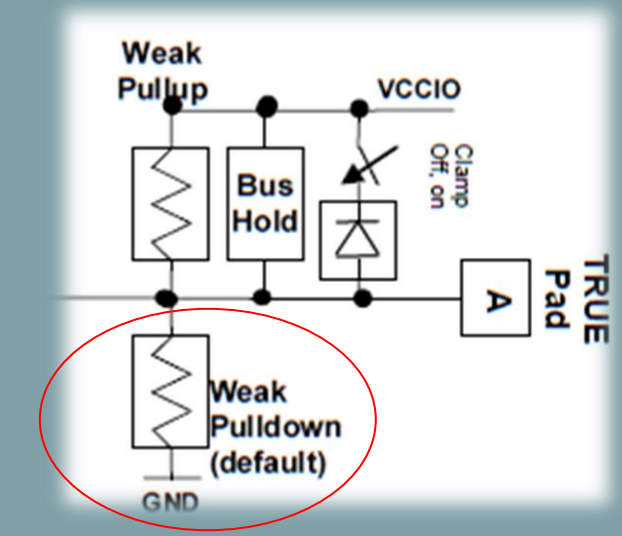
- Bridging support for high-resolution images
- Futureproof your designs for sensors and displays
- Coupled with increased EBR for improved image sharpness

MachXO4 has highest I/O count at 10k LUTs vs Competition (up to 382 pins)

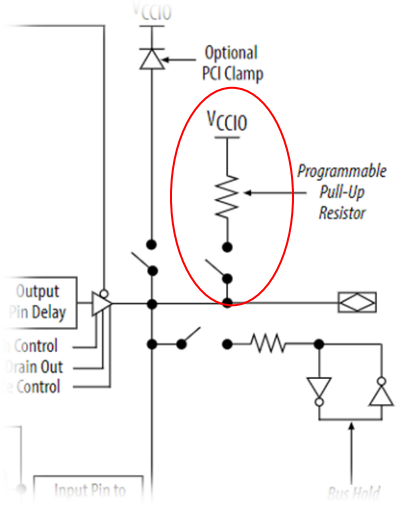
No “Shark-Fin” I/O

- I/O cell defaults to weak pull-down resistor during power-up
- **Key benefits**:
  - Ensures stable reset during power-up to avoid premature FPGA activation before power rails and clocks are stable
  - Prevents floating inputs
  - Reduced leakage current and power consumption

Lattice Semiconductor



Competition



Hot Socketing

- **Hot socketing** is the ability of an FPGA to plug into an active bus without damaging the device
- MachXO4 devices:
  - Default I/O to high-impedance state during power up
  - Minimize leakage current into I/O pins as low as 350 uA
  - Perform optimally in power supply management and how-swap applications

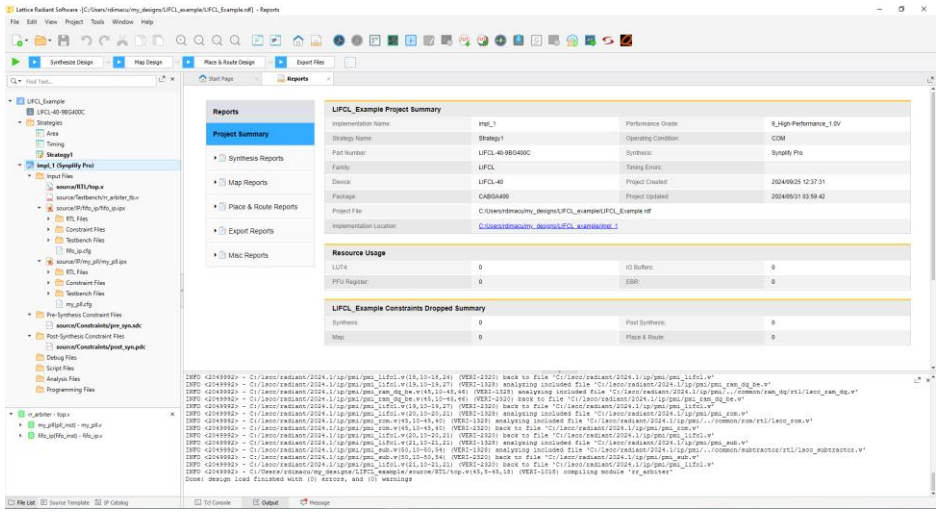
MachXO4 eliminates need for complex external protection circuitry

Low Static Power down to 1 mW

20+ Years of Product Longevity

Accelerated Design Productivity using Lattice Radiant Tool

LATTICE RADIANT DESIGN SOFTWARE



Several useful features such as Soft IP user interface, Physical Constraints, Floorplan View, Power Calculator, Programmer, Simulation Wizard, and Netlist Analyzer.

RTL Support. Industry Leading RTL language support for VHDL, VHDL-2008, Verilog, and SystemVerilog.

Synthesis Engine. User choice of synthesis solutions with industry leading Synplify Pro & Lattice Synthesis Engines.

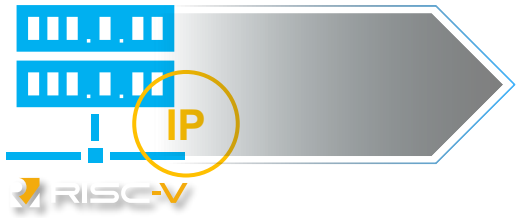
Advanced Scripting Capability. Fully scriptable command-line and TCL design flow.

State-of-the-Art GUI. Supports "one-click" compilation flow & cross-probing between analysis tools.

Timing Analyzer. Supports industry standard SDC (Synopsys Design Constraints) timing constraints.

Reveal. Embedded Logic Analyzer capability with debug on HW from RTL & post-synthesis stages.

Lattice Propel – The Easy FPGA Processor Design Environment



Lattice Propel Builder
IP System Integration

Complete Set of Graphical and Command-line Tools

Lattice Propel SDK
Industry-standard Software Development

Software Libraries and Board Support Packages
Build, Compile, Analyze, Debug

LATTICE DESIGN TOOLS

Intuitive, Easy-to-Use, Powerful

MACHXO4 MARKET SOLUTIONS

INDUSTRIAL

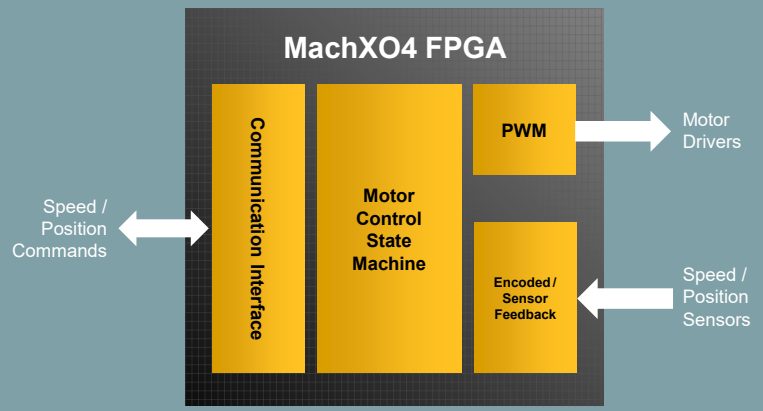
ROBOTICS

VISION

EDGE AI

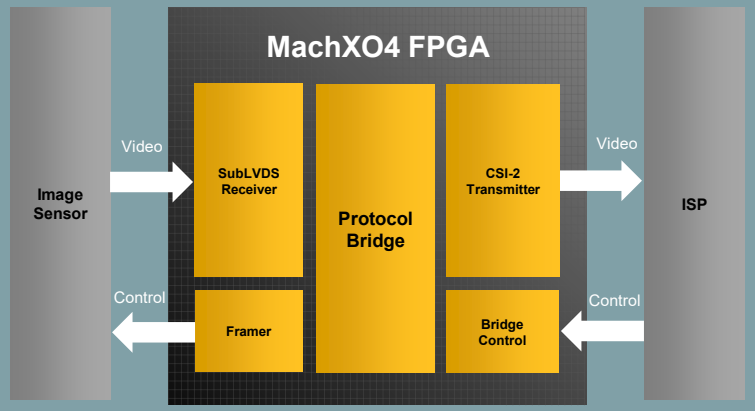
MachXO4 Example Use Cases

Motor Control



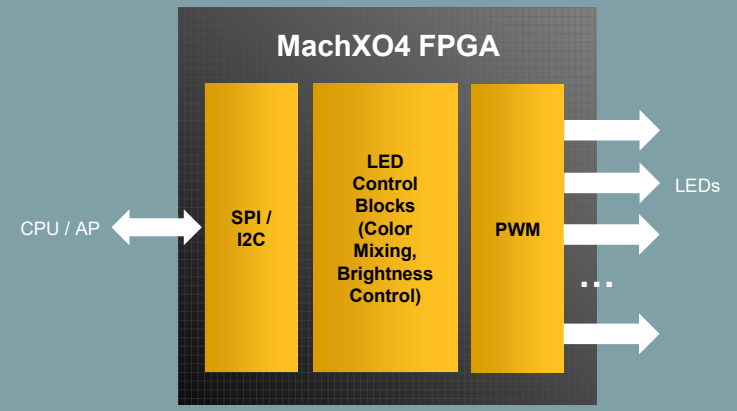
- Support for various motor types across industrial, automotive, and embedded systems
- IGBT protection and SPI for real-time MCU feedback
- Low-power, fast-response communication standard compatibility
- Small footprint

Camera & Display Bridging



- Supports 1–4 CSI-2 lanes up to 900 Mbps (Rx/Tx)
- DSI Tx with HS and LP modes (Tx/Rx)
- Compatible with RAW, YUV, RGB, YCbCr, and user-defined formats
- Compact package: Fits in 36-WLCSP (2.5 × 2.5 mm)

LED Control



- Programmable I/O and PLL for dimming, blinking, and color mixing
- Low power operation for efficient lighting
- Integrated Flash/UFM for storing LED profiles

More Resources Available

Sales Resources

- Sales Toolbox – Presentations by marketing team for customers
- MACHXO4 Early Access Program – Resources for Early Access Program customers

Lattice Insights On-demand Trainings

- Control & Security Product Line Overview (1 Hr 13 Min)
- Developing with Lattice FPGA: Advanced Security Features for Configuration (25 Min)
- Security Overview: Introduction to Lattice Sentry Solution & SupplyGuard (52 Min)
- Developing with Lattice Sentry Solution (25 Mins)

MachXO4

- Reference Design
- Example Use Cases
- Documentation

MachXO4 Migration Tool

- Software Tool
- Documentation


LATTICE
SEMICONDUCTOR
The Low Power Programmable Leader