



# **Radiant 2025.1 Tutorial CertusPro-NX Versa Board**

November 2025



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## Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

## Contents

Introduction .....	7
Learning Objectives.....	7
Time to Complete This Tutorial.....	8
System Requirements .....	8
Accessing Online Help.....	8
About the Tutorial Design .....	9
About the Tutorial Data Flow.....	9
Task 1: Create a New Lattice Radiant™ Software Project.....	11
Task 2: Create OSC component Using IP Catalog.....	17
Task 3: Verify Functionality with Simulation.....	20
Task 4: Inspect Strategy Settings .....	25
Task 5: Run Synthesis Process.....	27
Task 6: Set Timing and Location Assignments .....	29
Task 7: Run Map Design and Check Reports.....	32
Task 8: Running Place and Route .....	34
Task 9: Examine Post Place and Route Results .....	37
Task 10: Analyze Power Consumption .....	39
Task 11: Run Export Utility Programs .....	41
Task 12: Download a Bitstream to an FPGA .....	41
Task 13: Use Reveal Inserter to Add On-Chip Debug Logic.....	46
Task 14: Use Reveal Logic Analyzer to Perform Logic Analysis.....	51
Summary of Accomplishments .....	55
Recommended References .....	55

## Table of Figures

Figure 1: Hands-On design block Diagram.....	7
Figure 2: Tutorial Data Flow.....	8
Figure 3: Lattice Radiant™ Software Design Environnement.....	10
Figure 4: New Project wizard (Project name & directory setting).....	11
Figure 5: New Project wizard (Add source files).....	12
Figure 6: New Project Wizard Device Selector Dialog Box.....	13
Figure 7: Lattice Radiant™ project interface.....	14
Figure 8: Include files for simulation only.....	15
Figure 9: Process Toolbar and Task Detail View.....	15
Figure 10: Black Box Warning message.....	16
Figure 11: Top Menu IP Catalog shortcut.....	16
Figure 12: IP Catalog Wizard.....	17
Figure 13: Configuration Block of Module PLL.....	17
Figure 14: Check Generating Result Dialog Box.....	18
Figure 15: Top Menu simulation wizard shortcut.....	18
Figure 16: Simulation wizard.....	21
Figure 17: Lattice Radiant™ settings-Enable simulation file generation.....	19
Figure 18: Simulation Wizard-Add source files.....	20
Figure 19: Simulation wizard - summary.....	21
Figure 20: Questasim interface with simulation waveforms.....	22
Figure 21: Questasim-Add internal signals to waveform.....	22
Figure 22: Questasim - Restart simulation.....	23
Figure 23: Questasim - Run simulation.....	23
Figure 24: Questasim - cursor and zoom Tools.....	23
Figure 25: File List View, including Implementations and Strategies.....	24
Figure 26: Strategies - Synplify Pro settings.....	25
Figure 27: Lattice Radiant™ Flow - Synthesis.....	26
Figure 28: Synthesis Report.....	28
Figure 29: Pre-Synthesis Timing Constraint Editor.....	28
Figure 30: Device Constraint Editor.....	29
Figure 31: pin locking .pdc file.....	30
Figure 32: MAP Report.....	32
Figure 33: Physical Designer.....	35
Figure 34: Physical Designer-Cross Probing.....	34
Figure 35: Physical Designer Routing View.....	34
Figure 36: Timing Analyzer View.....	35
Figure 37: Timing analyzer - Waveform view.....	36
Figure 38: Timing Setting Dialog Box.....	37
Figure 39: Power Calculator.....	40
Figure 40: Design block Diagram.....	40
Figure 41: Lattice CertusPro-NX™ Versa board main components.....	41
Figure 42-Programmer interface.....	44
Figure 43: Device Properties Dialog Box.....	42
Figure 44: Lattice Programmer – Successful Programming.....	43
Figure 45: Evaluation Board - programmed.....	44

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<i>Figure 46: Reveal Wizard - Debug Stage</i> .....	45
<i>Figure 47: Reveal Inserter Main Window</i> .....	45
<i>Figure 48: Reveal Trigger Signal Setup Tap</i> .....	47
<i>Figure 49: Reveal Insert Debug to Design Dialog Box</i> .....	48
<i>Figure 50: File List with Reveal Debug File</i> .....	48
<i>Figure 51: Reveal Analyzer Startup Wizard</i> .....	50
<i>Figure 52: Reveal Analyzer Trigger settings</i> .....	51
<i>Figure 53: Reveal Analyzer waveforms</i> .....	52

## Introduction

The next generation design tool for FPGA design, Lattice Radiant™ software is designed to address the needs of high-density FPGA designs.

This tutorial leads you through all the basic steps of creating, processing, and analyzing HDL designs targeted to Lattice CertusPro-NX™ device family. It shows you how to use several processes, tools, and reports from the Lattice Radiant™ software to import sources, run design analysis, and inspect strategy settings. The tutorial then proceeds to step of examining the device resources, setting timing and location assignments, and editing constraints to implement the design to the target device. Finally, you have the option of downloading the generated bitstream to a development board and inserting a logic analyzer for debugging purposes.

## Learning Objectives

When you have completed this tutorial, you should be able to do the following:

- ▶ Create a new Lattice Radiant™ software project.
- ▶ Create a module using IP Catalog.
- ▶ Verify functionality with simulation.
- ▶ Inspect strategy settings.
- ▶ Examine resources.
- ▶ Set timing and location assignments.
- ▶ Run synthesis.
- ▶ Run map design and check reports.
- ▶ Run place and route.
- ▶ Examine post place and route results.
- ▶ Analyze power consumption.
- ▶ Run Export Utility programs & generate a bitstream.
- ▶ Download a bitstream to an FPGA.
- ▶ Use Reveal Inserter to add on-chip debug logic.
- ▶ Use Reveal Logic Analyzer to perform logic analysis.

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## Time to Complete This Tutorial

The time to complete this tutorial is approximately 2 hours.

## System Requirements

The following is required to complete the tutorial:

- ▶ Lattice Radiant™ software Version 2025.1 or Later
- ▶ (Optional) Lattice CertusPro-NX™ Versa Board to download a bitstream and to insert debug logic using Reveal Inserter.

### **Note**

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For more information on the CertusPro-NX Versa Board, refer to:

<https://www.latticesemi.com/products/developmentboardsandkits/certuspro-nx-versa-board>

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## Accessing Online Help

You can find online help information on any tool included in the tutorial at any time by choosing Help > Lattice Radiant™ Software Help.



## About the Tutorial Design

The design in this tutorial consists of a combination of HDL modules. The main function is to have a counter value displayed on the 7-Segment LED with counter direction (UP or DN). Multiple HDL modules are used to implement this design: Counter, 7-Segment display decoder and a simple display controller.

The target device used is Lattice CertusPro-NX™ on the Versa Board as shown in the block diagram below.

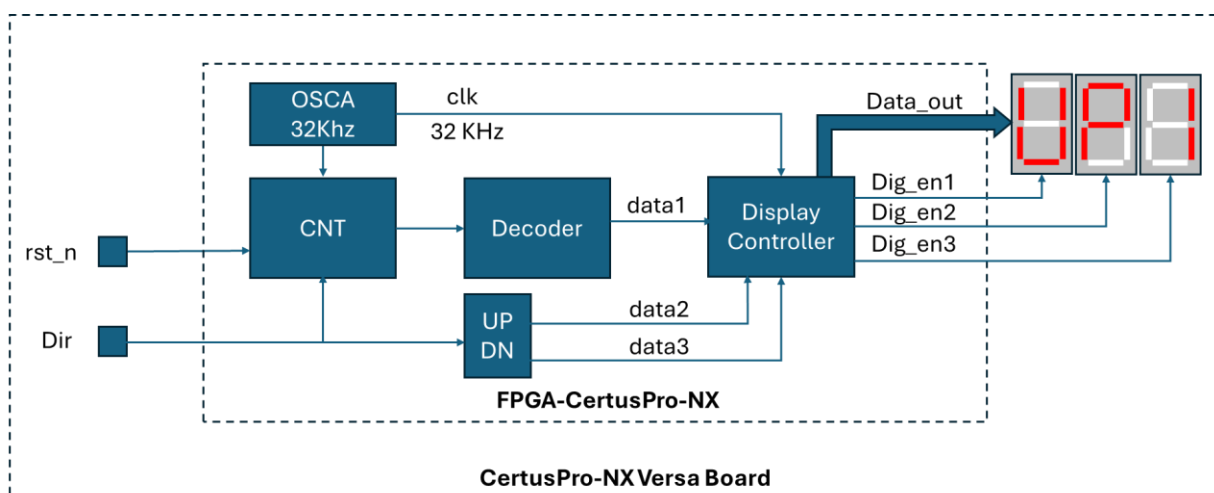


Figure 1: Hands-On design block Diagram

## About the Tutorial Data Flow

Figure 2 illustrates the tutorial data flow through the FPGA design system. You may find it helpful to refer to this diagram as you move through the tutorial tasks.

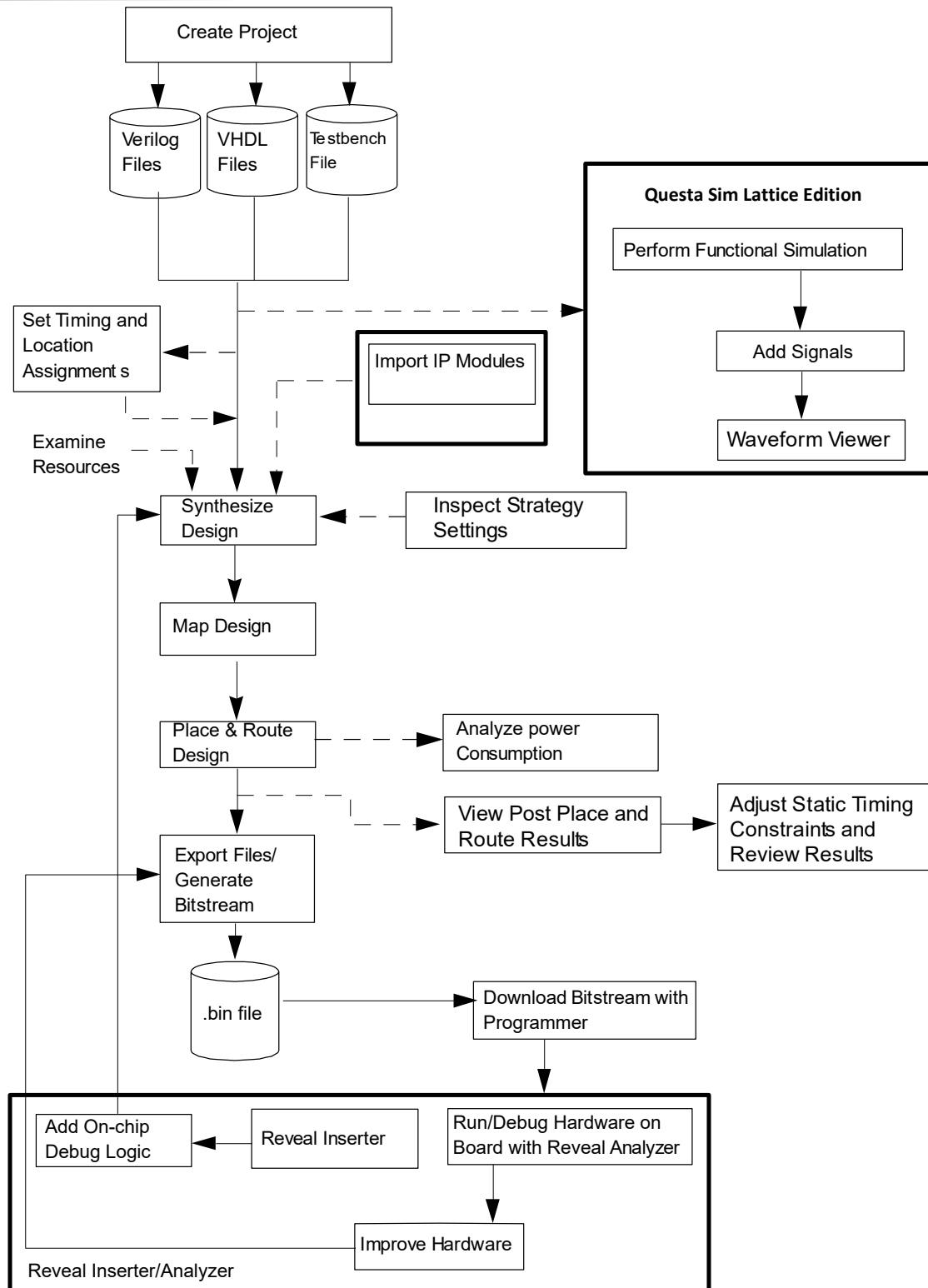


Figure 2: Tutorial Data Flow

## Task 1: Create a New Lattice Radiant™ Software Project

Projects are used to manage input files, constraints, and optimization options related to FPGA implementation. While there are several tasks you can perform independent of a project, most designs start with creating a new project.


### Note

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Some of the screen captures in this tutorial may have been taken from a version of Radiant software that differs from the one you are using. There may be slight differences in the graphical user interface (GUI), but the software functions are the same.

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### To create a new project:

1. Do one of the following depending on your operating system:
  - ▶ On Windows, go to the Start menu and choose Lattice Radiant™ Software >  Radiant Software.
  - ▶ On Linux, enter the following on a command line:

`<install_path>/bin/linux64/Radiant`

The Lattice Radiant™ Software Design Environment appears, as shown in Figure 3.

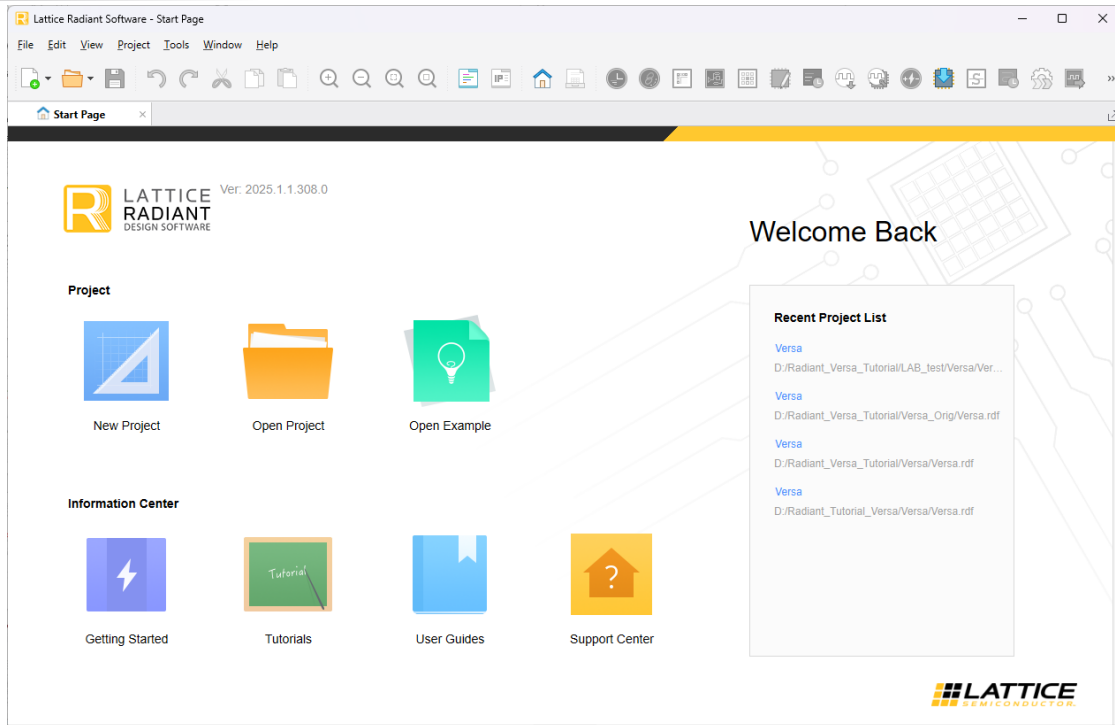



Figure 3 : Lattice Radiant™ Software Design Environnement

The initial layout provides the Start Page, which provides a list of common project actions like New Project to run the New Project wizard, Open Project to open a pre-existing project, and Open Example.

Refer to Lattice Radiant™ online Help to get answers for most questions, it is a good starting point. It describes the FPGA design flow using Radiant software, the libraries of logic design elements, and the details of Radiant software design tools. The Help also provides easy access to many other information sources. The Help can be accessed from Help > Lattice Radiant Software Help.

2. Open a new project in one of the following ways:

- ▶ On the Start page, click the New Project  button.
- ▶ From the Lattice Radiant™ software main window choose File > New > Project.

The New Project wizard opens.

3. Click **Next**.

4. Specify the project name: **Versa**.

### Note

File names for Radiant software projects and project source files must start with a letter (A-Z, a-z) and must contain only alphanumeric characters (A-Z, a-z, 0-9) and underscores (\_).

5. Click **Browse**. In the Project Location dialog box, browse to where you want to store the project's files, such as D:/Radiant\_Versa\_Tutorial, as shown in Figure 4. Click **Select Folder**.
6. Leave the Implementation Name as the default: impl\_1. The directory to store the implementation is automatically displayed in the Location box. We will talk about creating a new implementation later in this tutorial.

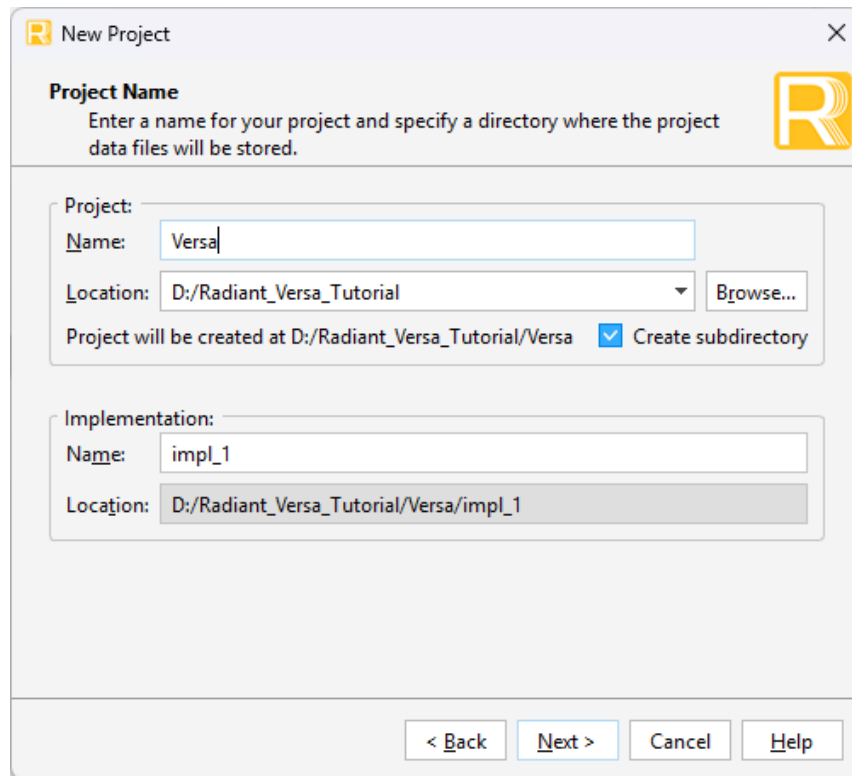


Figure 4: New Project wizard (Project name & directory setting)

7. Click **Next**.

The Add Source dialog box appears.

8. Click **Add Source**.

The Import File dialog box appears.

9. Navigate to the folder containing the source files (part of the training package), select the source files in the directory and click on open, you should see all files added like below:

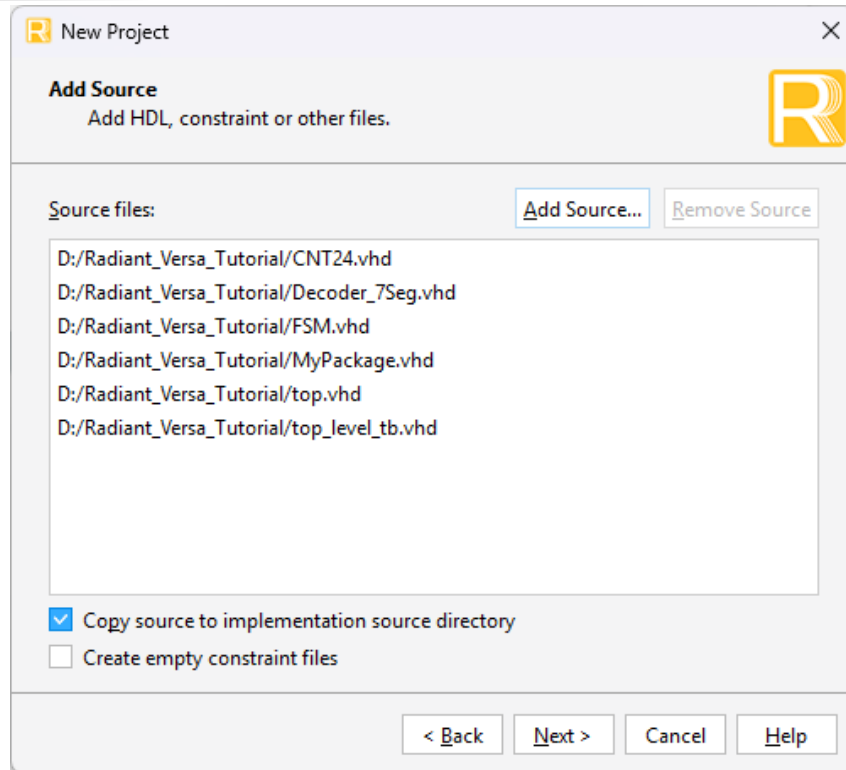


Figure 5: New Project wizard (Add source files)

Make sure “Copy source to implementation source directory” is checked.

Clear “Create empty constraint files”. This option is not required for this tutorial.

10. Click **Next**.

The Select Device dialog box appears.

11. Select the following device options:

- ▶ Family: **LFCPNX**
- ▶ Device: **LFCPNX-100**
- ▶ Operating Condition: **Commercial**
- ▶ Package: **LFG672**
- ▶ Performance Grade: **9\_High-Performance\_1.0V**

The dialog box should resemble Figure 6. The Device Information box on the right-side shows (as applicable) the supported Voltage, LUTs, Registers, EBR Blocks, DSPs, PLLs, DLLs, PCSs, PIO Cells, and PIO Pins.

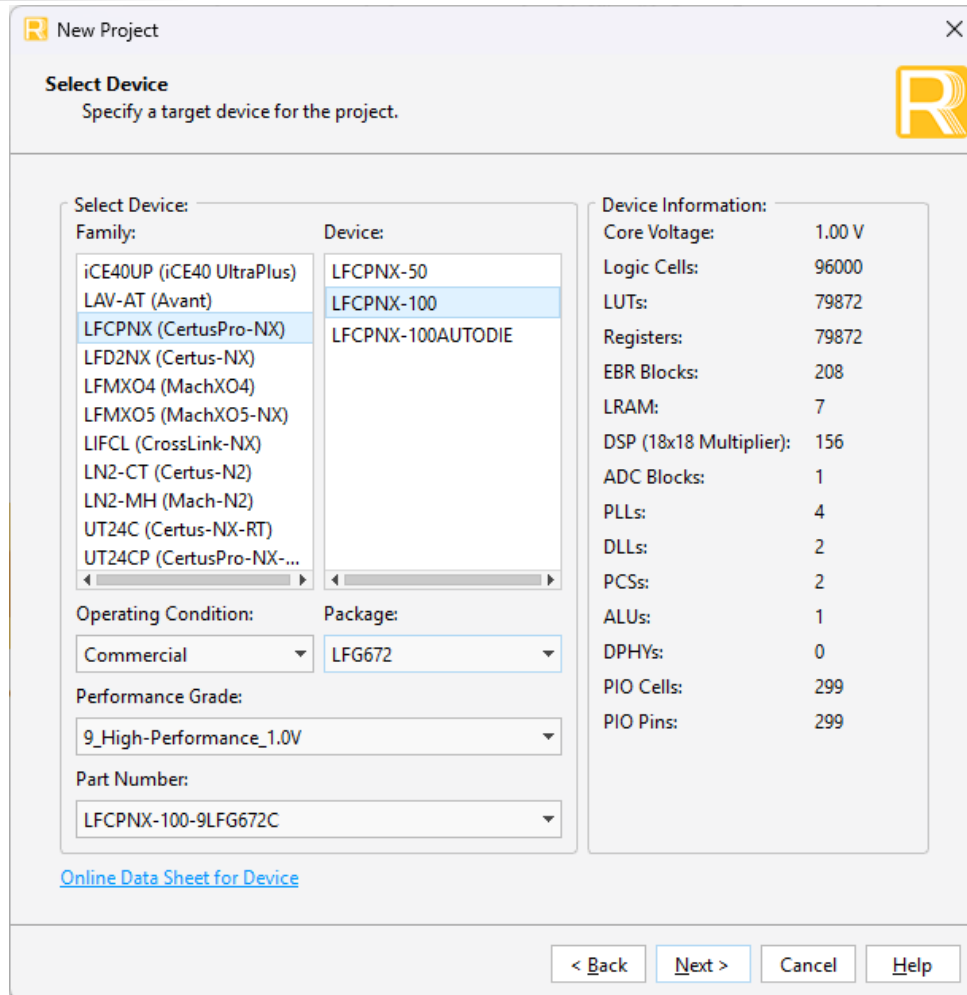


Figure 6 : New Project Wizard Device Selector Dialog Box

12. Click **Next**.

The Select Synthesis Tool dialog box opens.

13. Select **Synplify Pro**.

14. Click **Next**.

The Project Information dialog box appears. The project information includes project name, location, implementation name, device, synthesis tool, and import source.

15. Click **Finish**.

The File List view (left side of screen) is populated, and the Reports view (right side of screen) appears as shown in Figure 7.

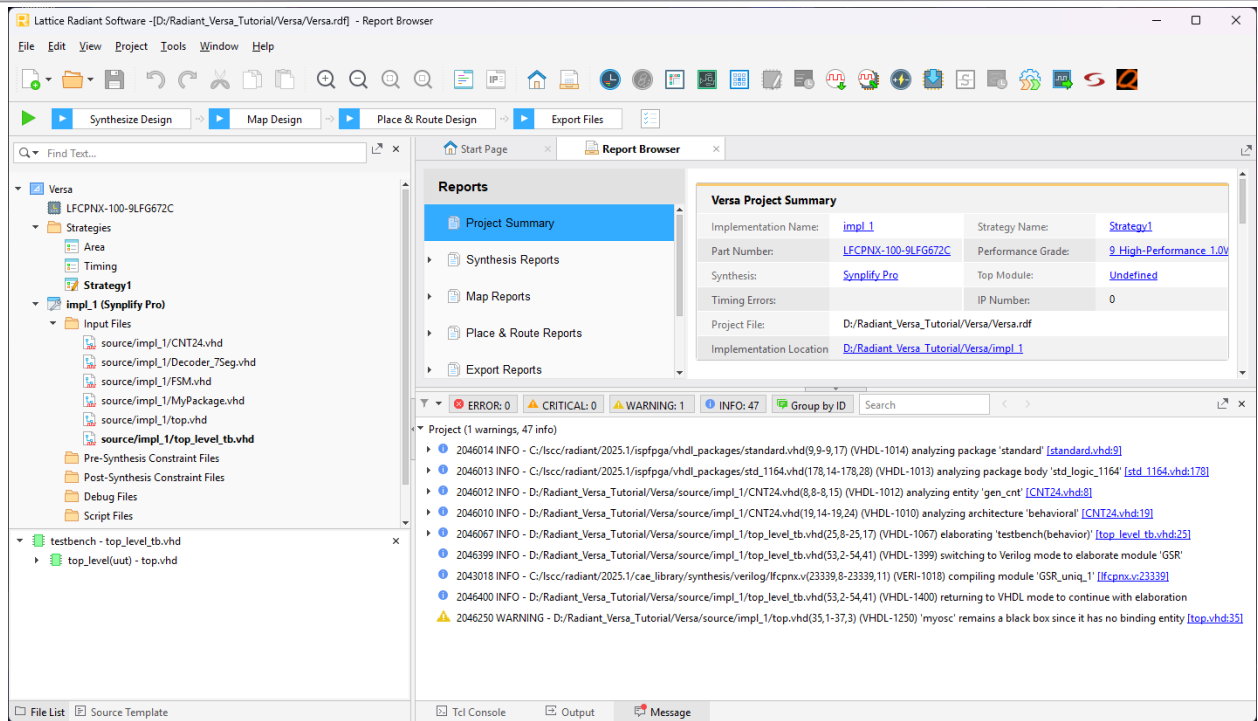


Figure 1: Radiant project interface

The File List view displays the components of the project. File List organizes project files by categories: Strategies, and Implementation including Input Files, Constraint Files, Debug Files, Script Files, Analysis Files, and Programming Files. You may adjust the file order by dragging and dropping file names in the list. Properties of each file are accessed by right clicking the file and choosing Properties from the pop-up menu.

### Note

You can also see Area and Timing listed in the Strategies folder in the File List view. These are predefined strategies supplied by Lattice Semiconductor that solve a particular design requirement. For details of these predefined strategies, refer to Radiant online Help.

16. In the File List view, right-click `top_level_tb.vhd` and choose Include for > Simulation.



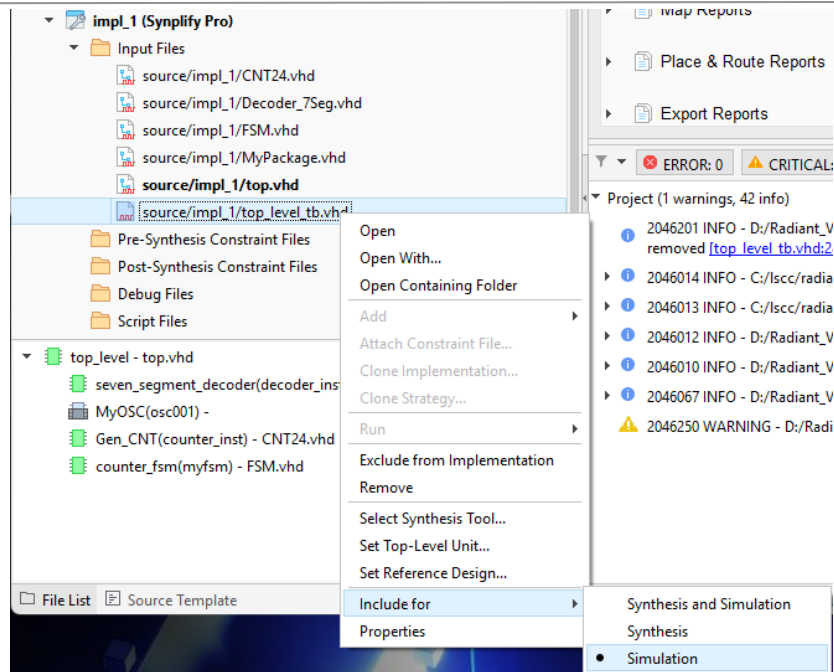


Figure 8: Include files for simulation only

17. The Process Toolbar lists all the processes available, such as Synthesize Design, Map Design, Place & Route Design, and Export Files. A process is a specific task in the overall processing of a source or project. You can view the processes available for a design in the Process Toolbar.


18. Click Task Detail View  to see detailed information about the processes.



Figure 9: Process Toolbar and Task Detail View

The Reports view allows you to examine and print process reports. There are two panes in the Reports view. The left pane lists the available reports. The right pane displays selected report details.

Log messages are displayed in the Output frame of the Lattice Radiant™ software's main window.

## Task 2: Create OSC component Using IP Catalog

IP Catalog is an easy way to use a collection of modules from Lattice Semiconductor. With IP Catalog, these modules can be extensively customized. They can be created as part of a specific project or as a library for multiple projects.

In this task, you will generate a component to enable an internal oscillator (OSC) module that is missing in the design. Notice the warning message when you imported source codes to the Lattice Radiant™ Project:

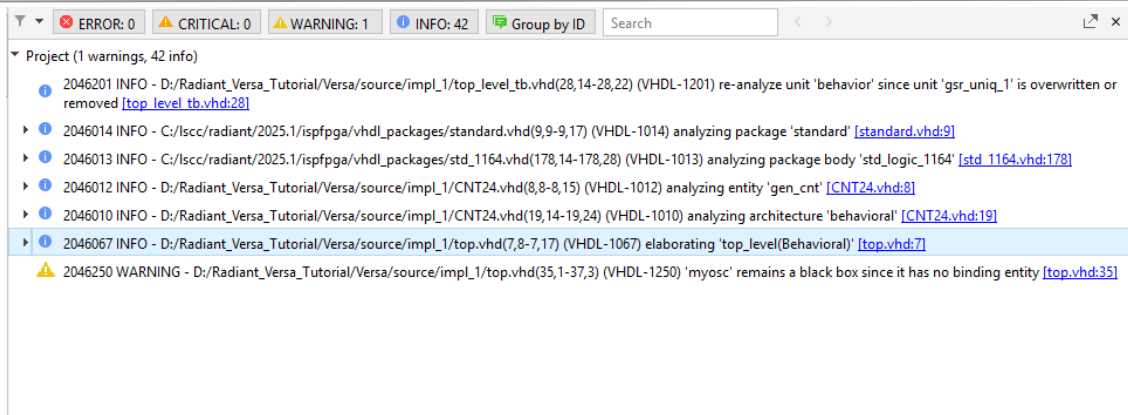


Figure 10: Black Box Warning message

This warning message is related to a missing component description that is used in the design (it is considered a black box by the software).

### To generate the OSC:

1. Open IP Catalog. IP Catalog is accessed via a tab at the lower left of the Lattice Radiant™ software or through the shortcut menu on the top of the interface as shown below. Click the icon to view the list of available modules and IP.



Figure 11: Top Menu IP Catalog shortcut

2. In the Module/IP on Local tree, open Module > Architecture\_Modules, and double-click OSC.
3. In the Module/IP Block Wizard, specify general project information and the base file name for the module or IP.
  - ▶ Instance Name is the base name for the module files (that is, with no extension). For this tutorial enter the name MyOSC.
  - ▶ The Create In box is the location for the customized module files. For this tutorial, use the default directory.

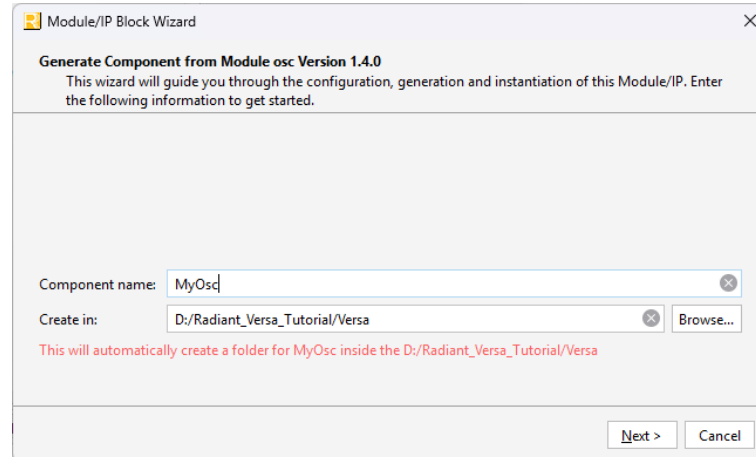


Figure 2: IP Catalog Wizard

4. Click **Next**.

The Module/IP Block Wizard dialog box opens.

5. In the dialog box, set the following like in Figure 13.

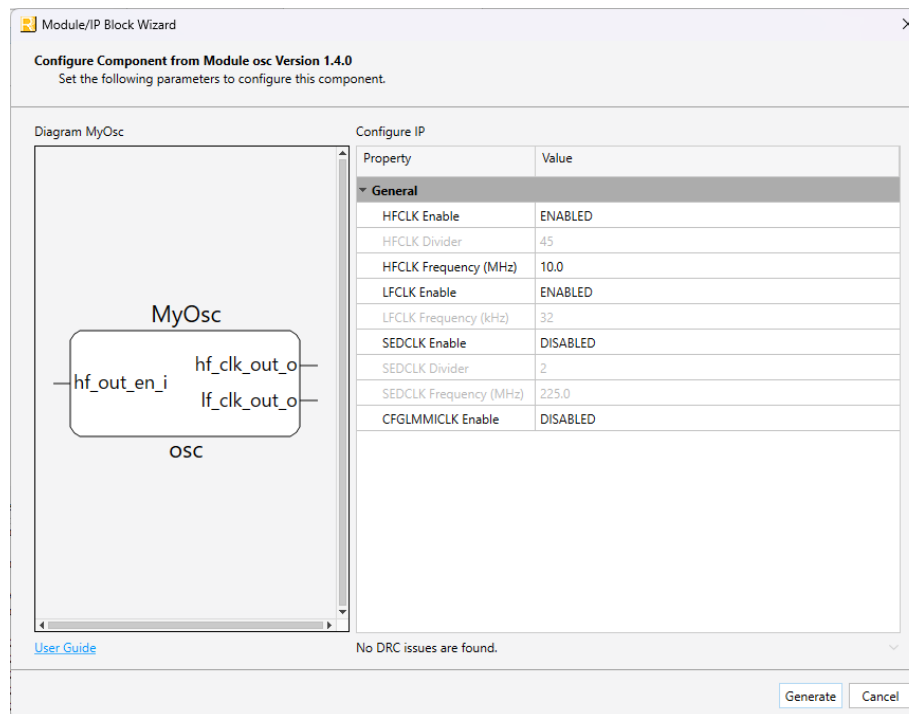


Figure 13: Configuration Block of Module OSC

6. Click **Generate**. The Check Generating Result dialog box should appear as shown in Figure 14.

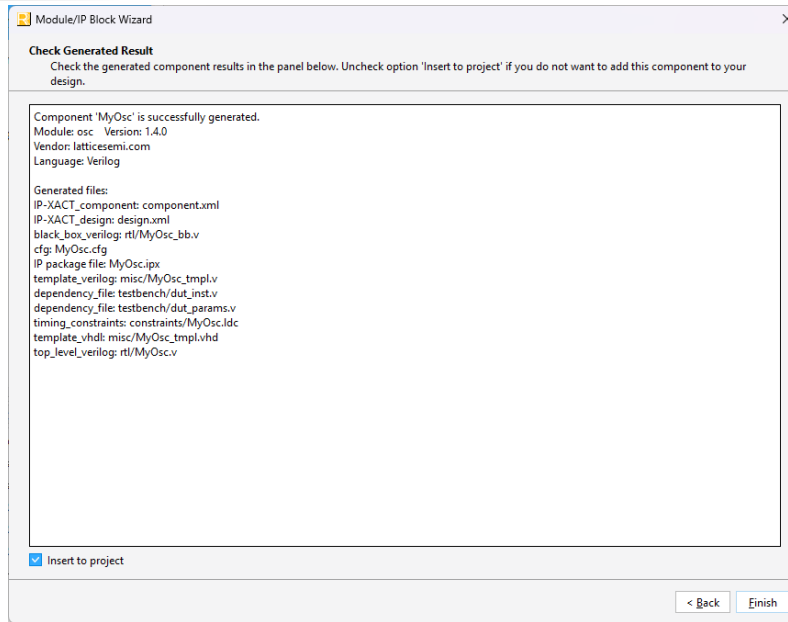


Figure 14: Check Generating Result Dialog Box

7. Make sure Insert to project is checked.
8. Click **Finish**.

### Task 3: Verify Functionality with Simulation

The Lattice Radiant™ software provides an interface to create a new simulation project file that can be imported into a standalone simulator.

Questasim® is an integrated simulation environment for VHDL, Verilog/SystemVerilog, EDIF, and SystemC designs.

In this task, you will simulate the design using Questasim® and analyze the resulting waveforms.

**Follow these steps to initiate and run the simulation of your design:**

1. Open simulation Wizard (Lattice Radiant™ integrated toll that helps setup environment and run the Use simulation)

On Lattice Radiant™ Project click on the simulation wizard as shown below or go to Tools > Simulation Wizard



Figure 15: Top Menu simulation wizard shortcut

2. Provide a simulation Project name (this will automatically create a script that allows you to re-run the simulation with same setup).

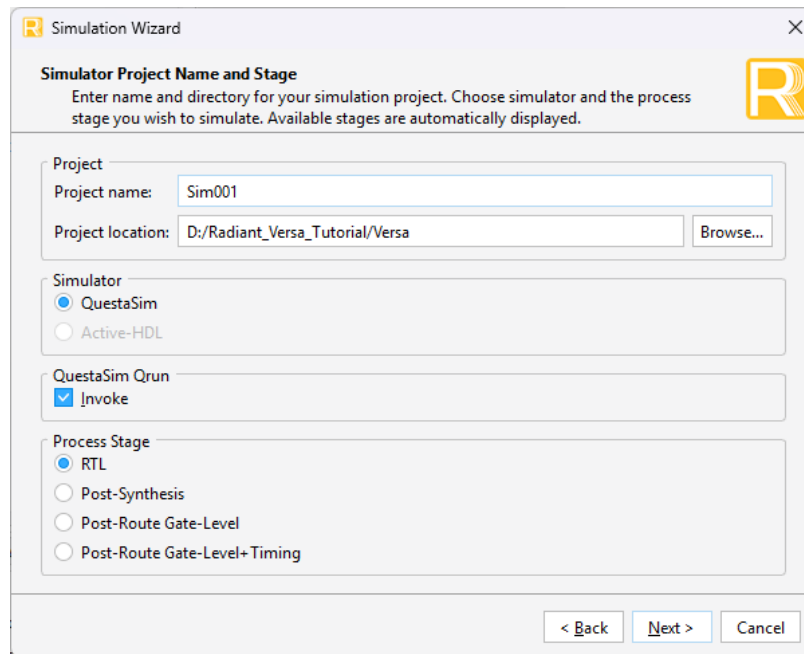


Figure 3: Simulation wizard

Multiple simulation options are available; we will run RTL simulation for this Tutorial. Click Next.

If you left the default for the project location, a dialog box opens saying, “simulation file does not exist. Do you want to create it?” Click Yes.

Note: To run Post-Synthesis simulation, make sure you enable Lattice Radiant™ options to generate required files.

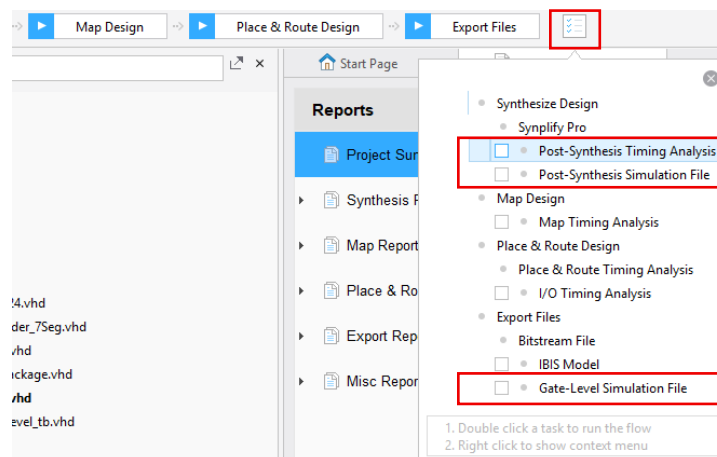


Figure 17: Lattice Radiant™ settings-Enable simulation file generation

3. Make sure you have the following files listed in the source file window and “Automatic set simulation compilation order” is checked. Then click Next.

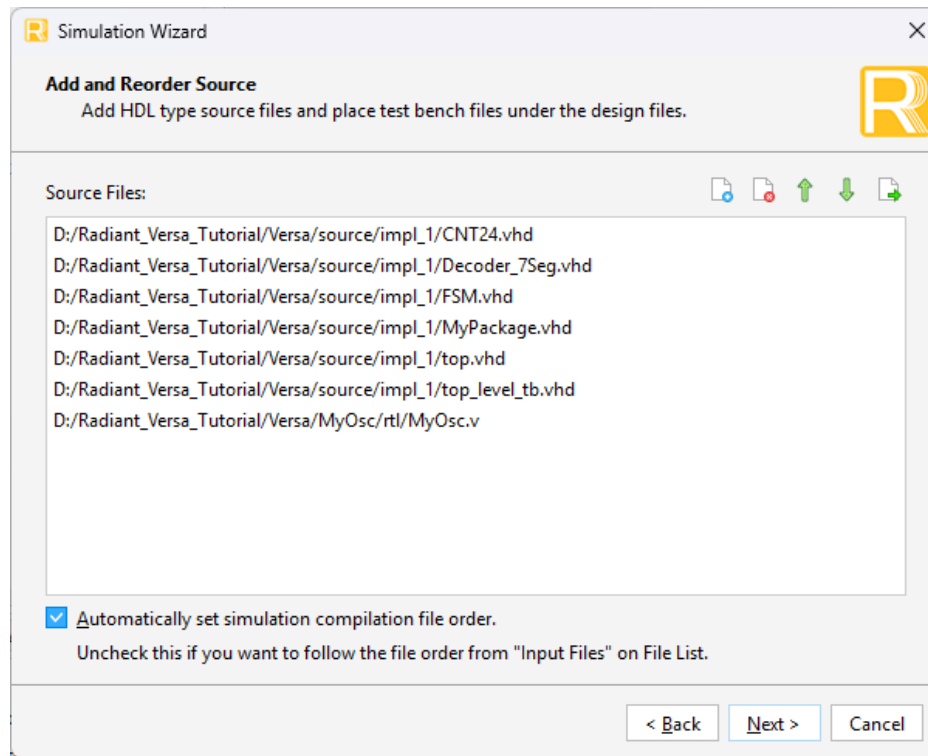


Figure 18: Simulation Wizard-Add source files

4. Click **Next**.
5. On Parse HDL files for simulation window click Next.

The Add and Reorder Source dialog box appears. Make sure all source files are present in the Source Files list. Leave the Automatically set simulation compilation file order option selected.

6. On Summary window make sure you have the following setting:
  - Launch Simulator GUI (**checked**)
  - Add top-level signals to waveform display (Checked)
  - Run simulation with default run of 1 ms
  - Design Optimization (**Checked**)
  - Simulator resolution: **fs**

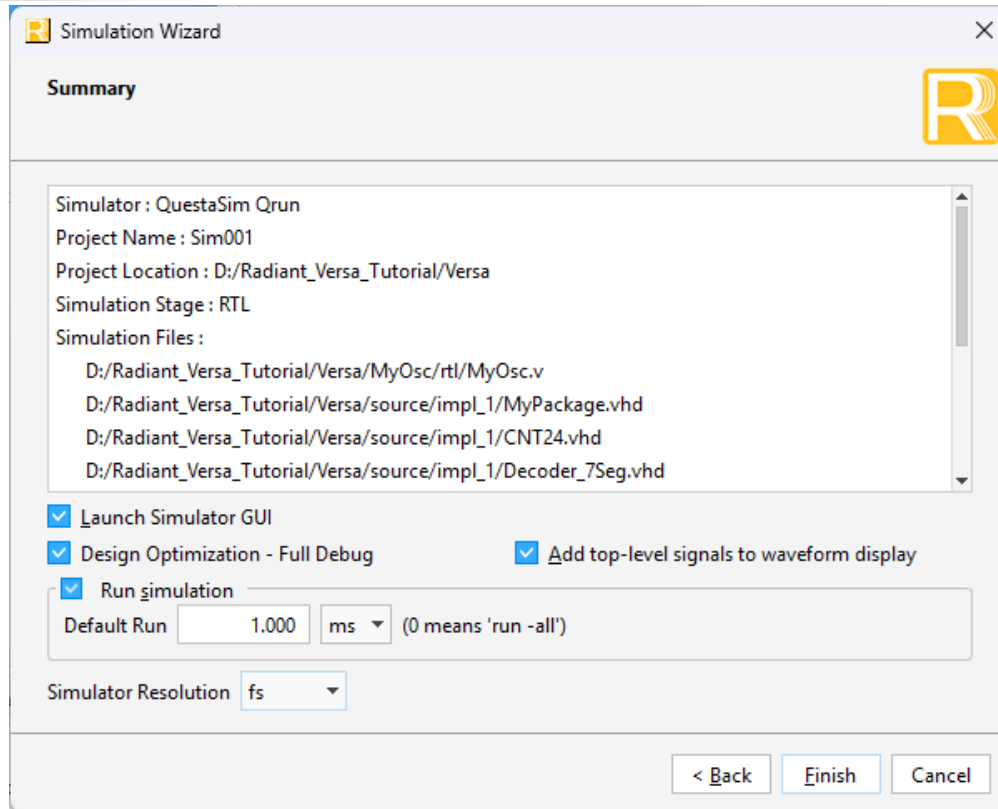


Figure 19: Simulation wizard - summary

7. Click **Finish**.

The Questasim software launches, and the simulation starts automatically. After completing the simulation, the waveform appears, as shown in Figure 20.

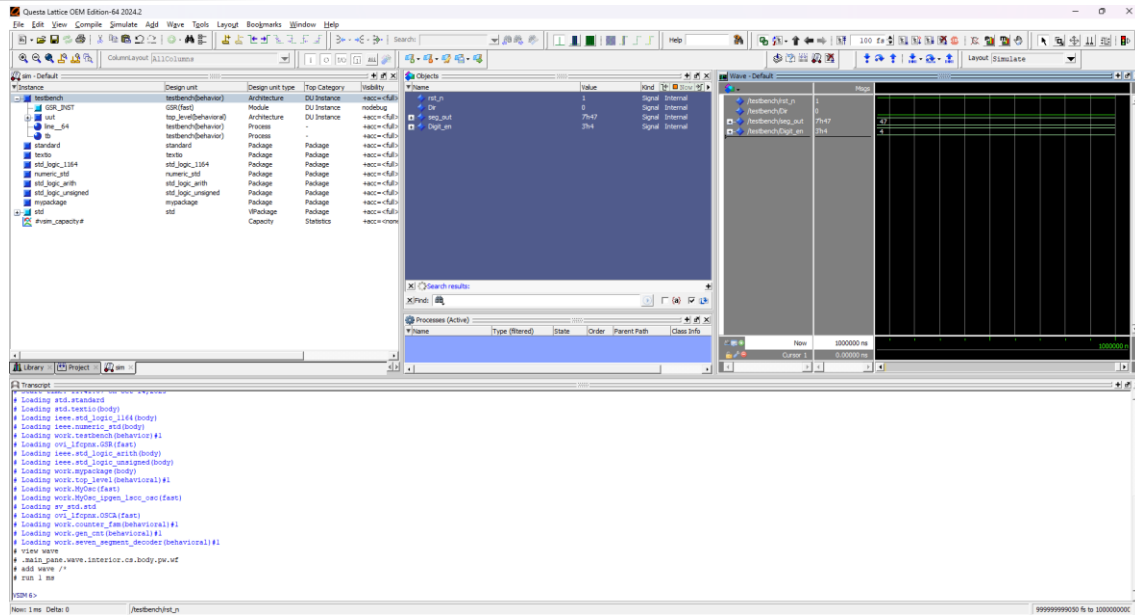


Figure 20: Questasim interface with simulation waveforms

## 8. Adding internal design signals to the waveform window:

In Questasim, click on MyFSM (under uut) in Instance window, then drag and drop state signal from object window to the waveform window. This will add FSM internal signals to the waveform window as shown below.

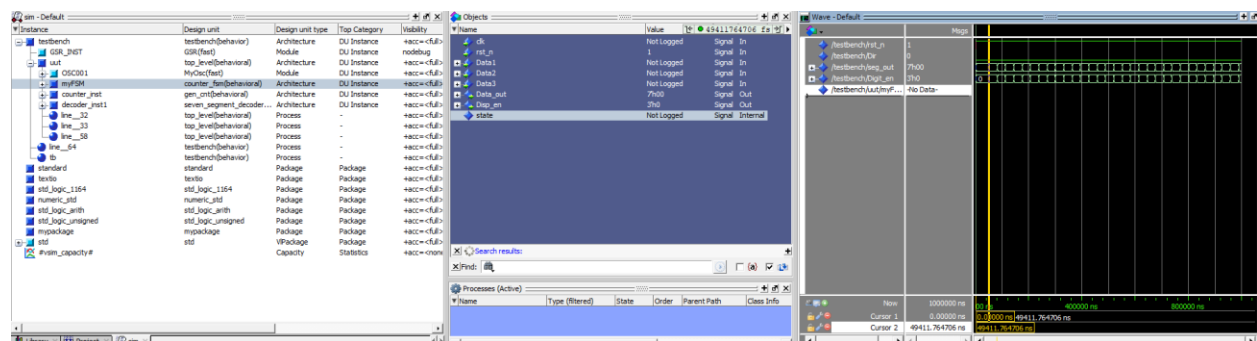


Figure 21: Questasim-Add internal signals to waveform

On the top menu, click on Simulate > Restart (click OK on popup window)

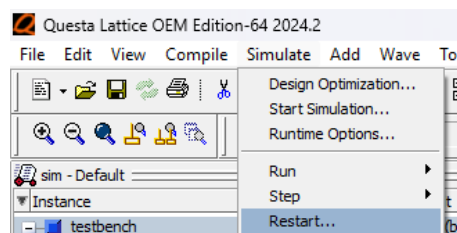


Figure 22: Questasim - Restart simulation



On the top menu change the time to 200 us then click on the Run icon as shown below to run the simulation.



Figure 23: Questasim - Run simulation



9. In Questasim, use the add cursor  or zoom tools  to have a focused view of the simulation and how waveforms are changing.



Figure 24: Questasim - cursor and zoom Tools

10. Choose File > Quit to close Questasim.

## Task 4: Inspect Strategy Settings

Implementations define the design of structural elements for a project, including source code, constraint files, and debug insertion. Implementation contains all source files, constraint files, debug files, scripts, and analysis files.

A strategy is a collection of tools settings for the different stages of the implementation process (synthesis, map, place & route, and so on). Strategies can control whether the design is optimized for area or speed, Synthesis settings, MAP and PAR settings, and many other factors. The Lattice Radiant™ software provides a default strategy, which should be a good collection of settings as a starting point, that can be tuned if needed.

You can modify Strategy1 as shown in the Strategies section in Figure 25 and create other strategies to experiment with or to use in different circumstances. Predefined strategies can also be cloned and then modified.

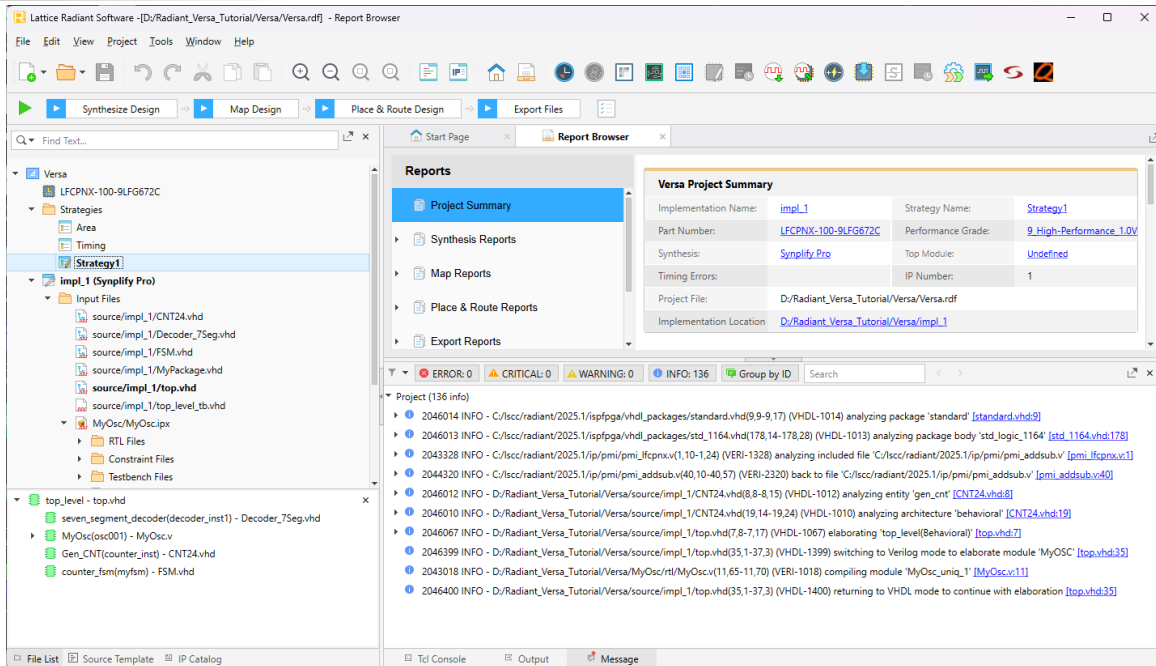


Figure 25: File List View, including Implementations and Strategies

### To view synthesis settings:

1. In the File List view, double-click Strategy1.

The Strategies - Strategy1 dialog box, shown in Figure 26, appears.

1. Click Synthesize Design > Synplify Pro.

A set of default global synthesis timing constraints and optimization settings appears in the panel. Synplify Pro settings are displayed as the default values in the dialog box.

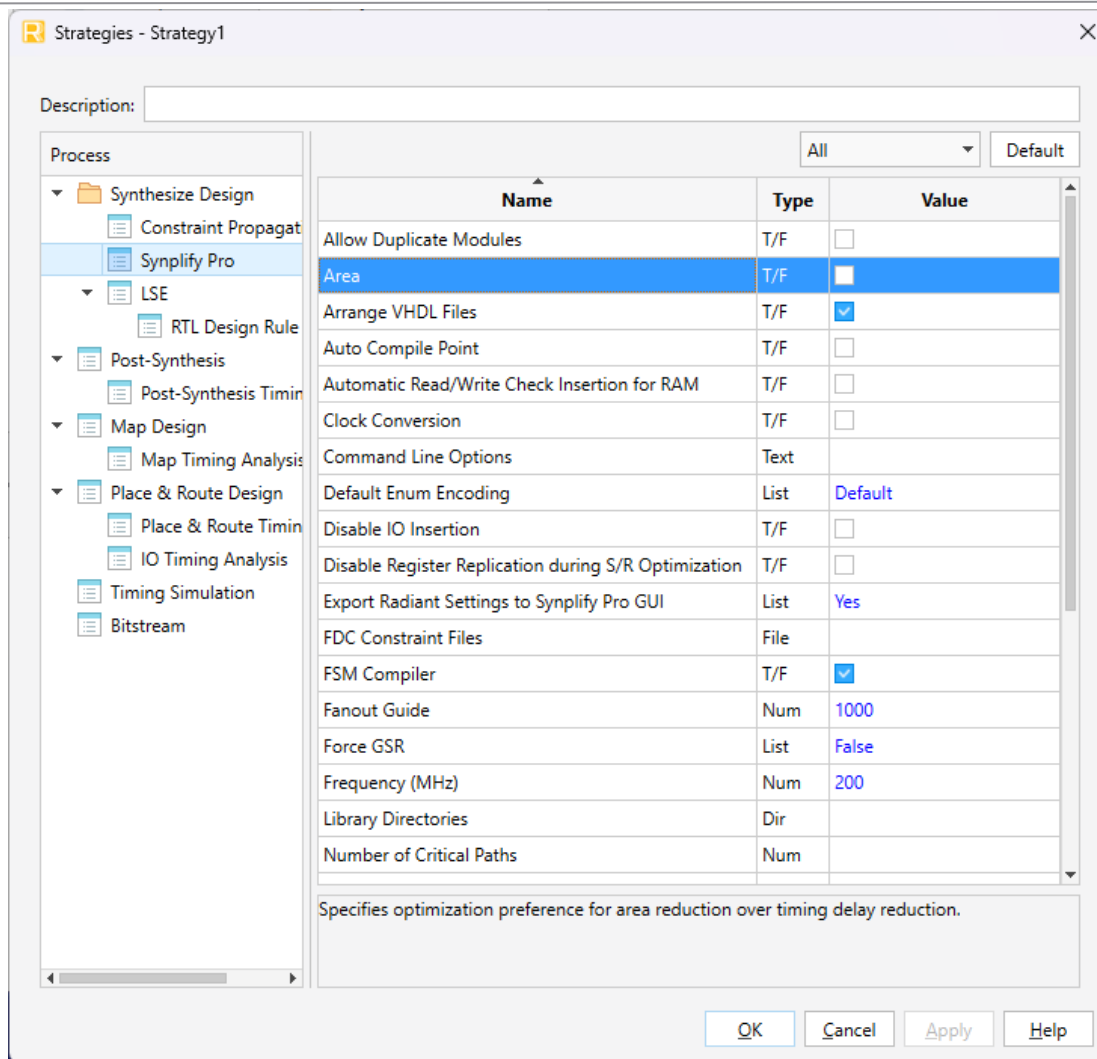


Figure 26: Strategies - Synplify Pro settings

For each option selected, descriptive text appears in the lower panel of the dialog box. Default values in the strategies dialog box are shown in blue while changed values are shown in black.

Click Cancel to close the Strategies dialog box.

## Task 5: Run Synthesis Process

Synthesis is the process of translating HDL files into a process-specific, gate-level netlist that is optimized for Lattice Semiconductor FPGAs. The Lattice Radiant™ software can be used with almost any synthesis tool.

The Lattice Radiant™ software comes with two fully integrated tools: Synopsys Synplify Pro for Lattice and Lattice Synthesis Engine (LSE). “Fully integrated” means that you can set options and run synthesis entirely from within the Radiant software.

In this Tutorial, you will use Synplify Pro to synthesize your design for the Lattice CertusPro-NX™ FPGA.

## To synthesize the design and examine resource utilization:

1. From the Process Toolbar, click Synthesize Design.

Task Detail View opens and tracks completion of the processes.

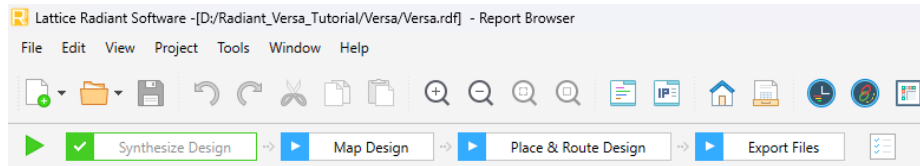




Figure 27: Lattice Radiant™ Flow - Synthesis

2. When the process is completed, look at the icon next to Synthesize Design. A green check mark  indicates success; a red X  indicates failure.
1. To view post-synthesis resource usage, click View > Reports, or click the Reports tab. The Synthesis report is displayed, as shown in Figure 28. Note that your Synthesis report results may differ slightly from what is shown in the example.

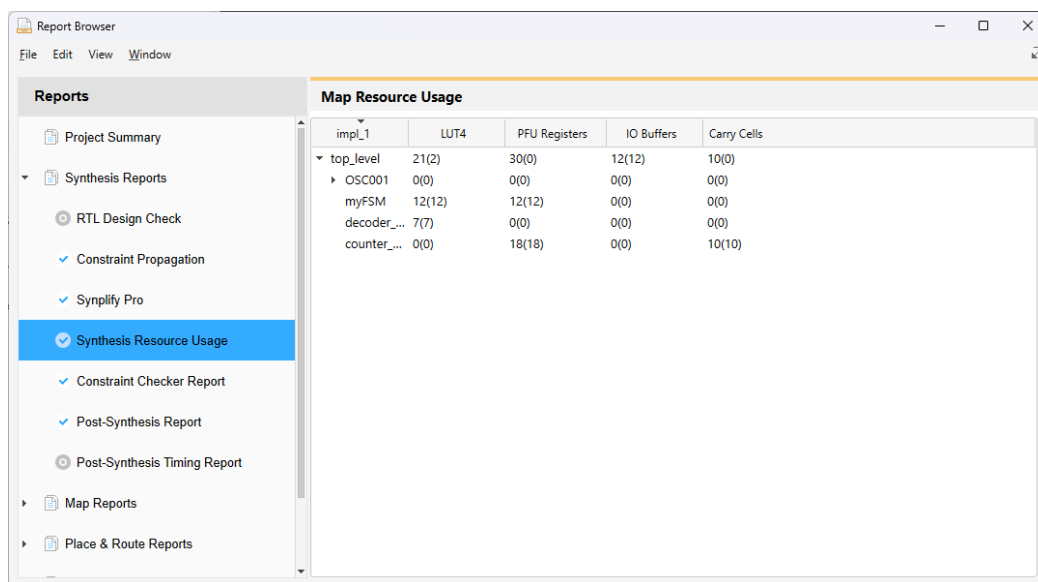


Figure 4: Synthesis Report

Note that the synthesis report integrates multiple sections: Synplify Pro log file, Synthesis Resource Usage, Post-Synthesis Report, and Post-Synthesis Timing reports, etc.

The Resource Usage table displays the number of logical resources within each hierarchical level of the design.


- LUT4 represents the total LUT4 count utilization throughout the design.

- ▶ PFU Registers represent the total PFU register utilization throughout the design.
- ▶ I/O Buffer scores the total number of I/Os in the design.


## Task 6: Set Timing and Location Assignments

Timing and location assignments apply logic synthesis, as well as backend map, and place-and-route tool to help meet your design requirements. A well-constrained design helps optimization algorithms work as efficiently as possible. In this section, you'll set default timing constraints for the operating frequency then assign package pins to specific I/O signals.

### To set timing constraints:

1. From the Tools menu, choose Tools > Pre-Synthesis Timing Constraint Editor, or click the shortcut  icon on the Lattice Radiant™ software toolbar. Make sure to choose Pre-Synthesis Timing Constraint Editor. For reference: Post-synthesis constraints impact design implementation after synthesis whereas Pre-synthesis constraint has an impact on the synthesis process.

The Pre-Synthesis Timing Constraint Editor appears. The top half is a spreadsheet with different tabs, each with rows of constraints that may want to add. The bottom half represents the SDC text syntax for constraints entered.

2. Click the Detach Tool icon  at the upper-right corner to detach the tool.
3. Click the **Clock** tab.
4. Double click on Object clock case and Click on the 3 dots to select the clocks available
5. A pop-up window appears, filter by object type: CLOCKNET
6. Select clk2 and click on OK
7. Click in the Frequency cell and enter 50 MHz as shown in Figure 29.

The Period column is calculated automatically and changes to 20 ns.

Note that in the text part of the view, the create clock constraint will be shown as below:

```
create_clock -name {clk2} -period 20 [get_nets clk2]
```

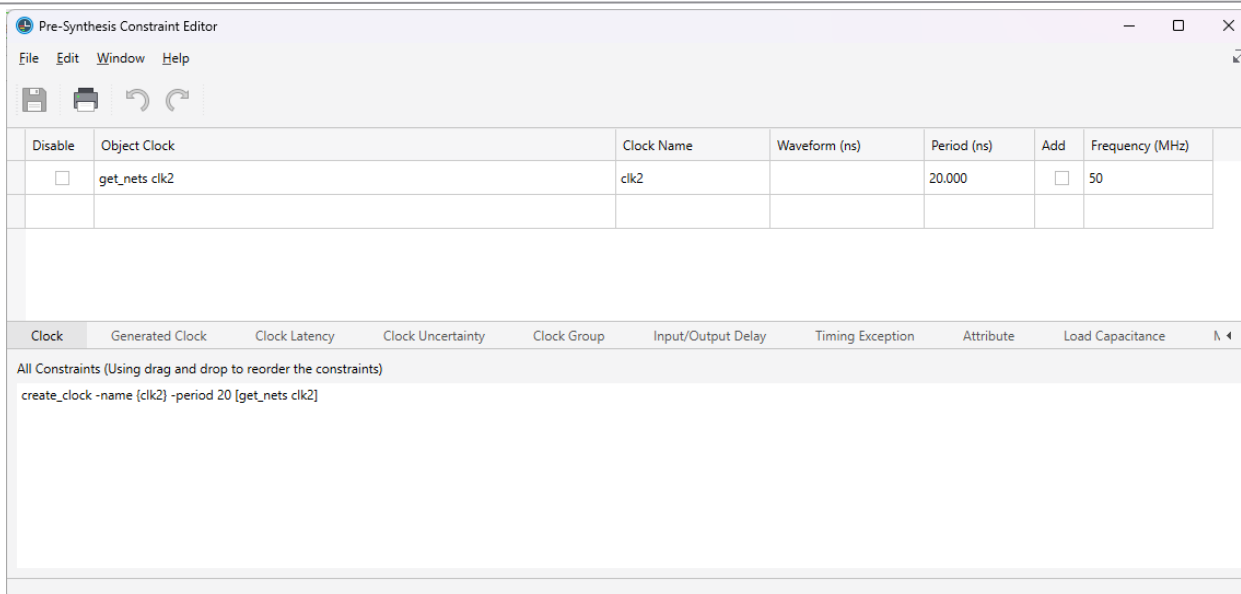



Figure 29: Pre-Synthesis Timing Constraint Editor

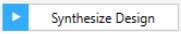
8. Choose **File > Save** timing\_constraints.sdc.
9. Close the Pre-Synthesis Constraint Editor.
10. In the File List view of the Lattice Radiant™ software main window, double-click the timing\_constraints.sdc file under Pre-Synthesis Constraint Files.


Source Editor appears with the .sdc file. Note the timing constraints defined so far.

11. Close the Source Editor.


### To set location constraints:

Device Constraint Editor is used to edit .pdc constraints file. The constraint editing GUI is available from the Lattice Radiant™ software toolbar  and Tools menu. All modified constraints will be saved to a .pdc file. The Device Constraint Editor shows the pin layout of the device and displays the assignments of signals to device pins.

Since we have changed pre-synthesis timing constraint, we need to update the synthesis phase Before opening Device Constraint Editor (Double click on  to run synthesis)

From Tools menu, choose Tools > Device Constraint Editor or click  on the Lattice Radiant™ software toolbar.

Device Constraint Editor appears.

1. Click Detach Tool icon  at the upper-right corner to detach the tool as shown in Figure 30.

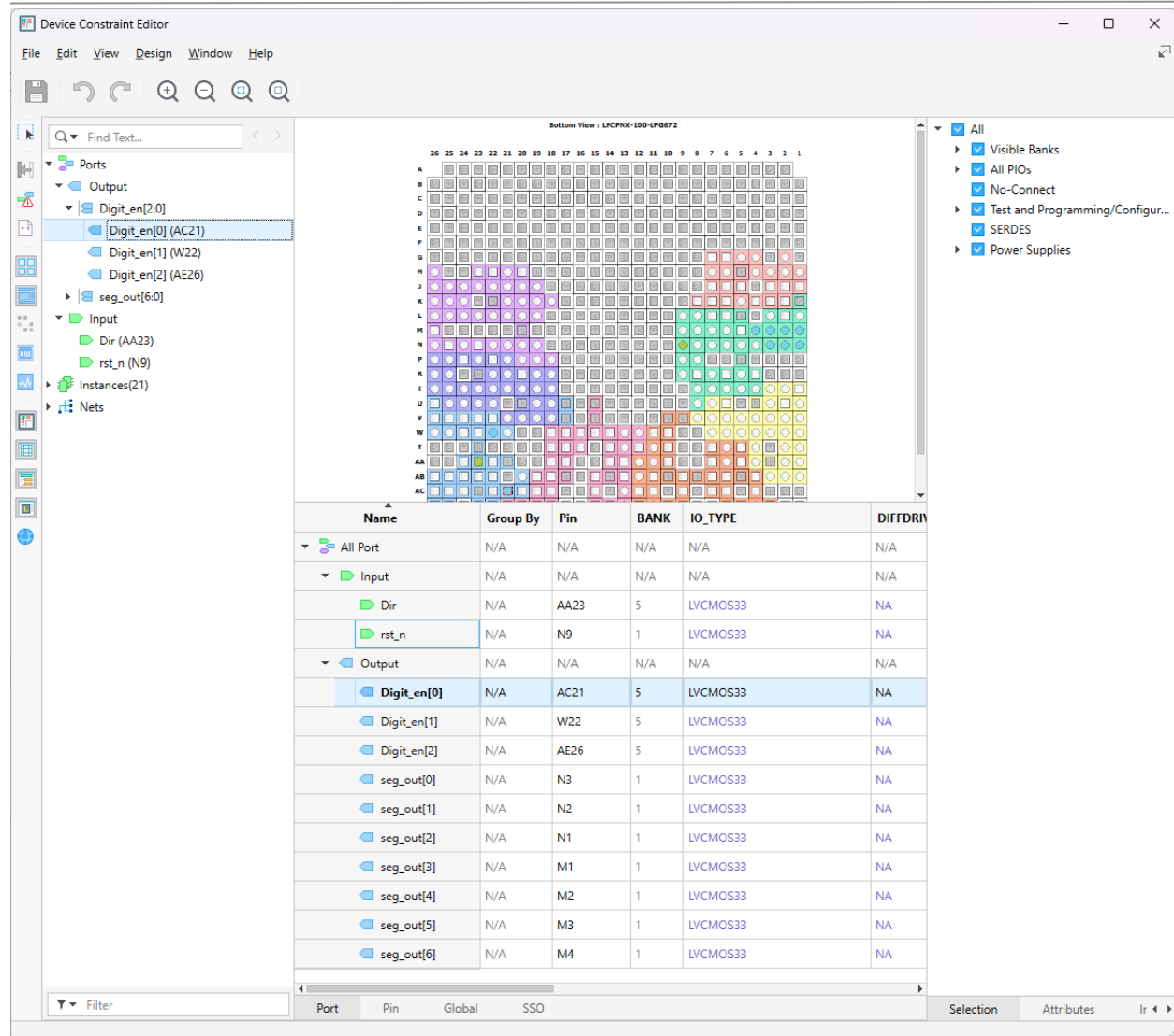


Figure 5: Device Constraint Editor

2. Select the Port tab, in the lower left of Device Constraint Editor.

Cell entries in Device Constraint Editor are color-coded to indicate the source of a constraint setting:

- ▶ Black - User-defined setting.
- ▶ Blue - Default.
- ▶ Green - Implied by the synthesis-defined constraint setting.
- ▶ Yellow - Implied by another user-defined setting.

3. Enter pin numbers as shown in Figure 30

Pin could be entered by writing the pins numbers directly to the spreadsheet view or by drag and drop from the port list to the package view.

#### 4. Save constraints

**File>Save** <directory name>\MyPDC.pdc

This step will allow you to save all the pin constraints entered into MyPDC.pdc text file (Post Synthesis Constraint file). You can open the text file from the Lattice Radiant™ files menu by double clicking on it as shown in Figure 31.

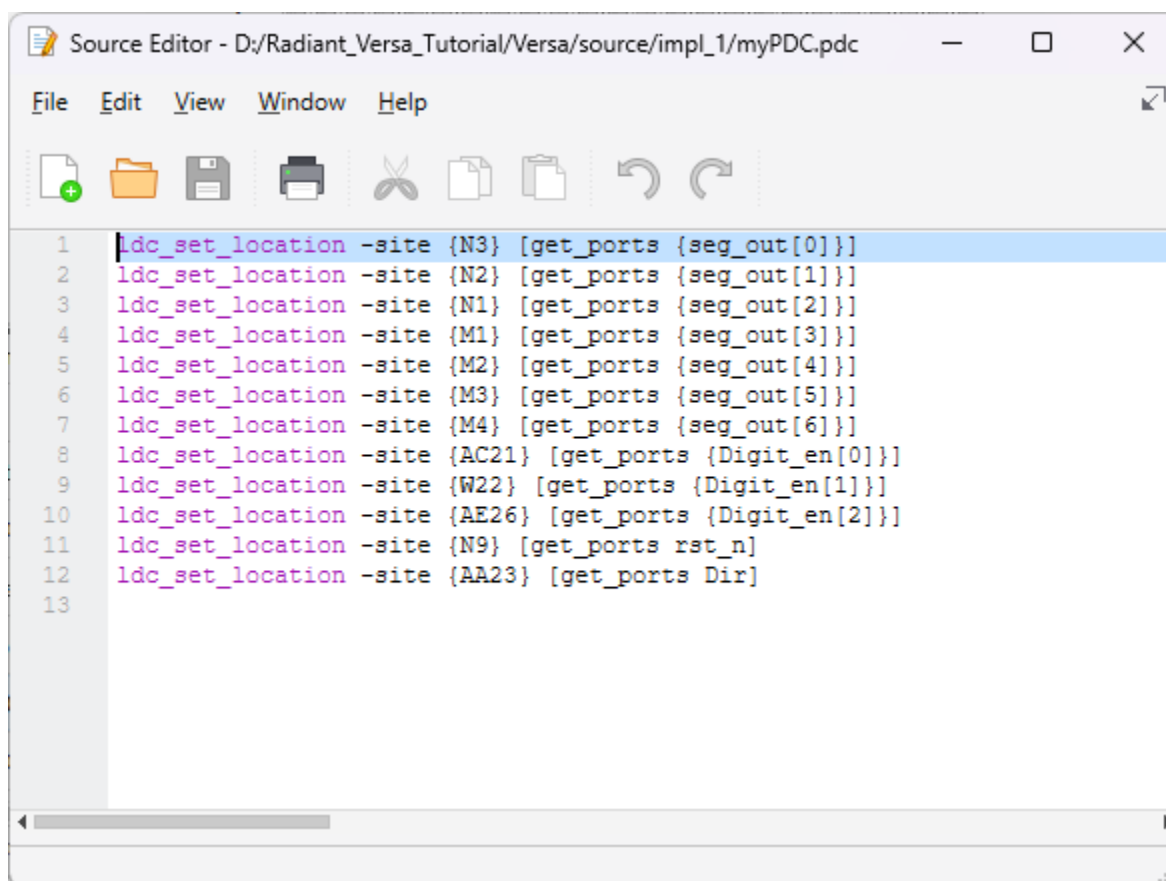


Figure 31: pin locking .pdc file


#### 5. Close Device Constraint Editor.



## Task 7: Run Map Design and Check Reports

Mapping is the process of converting a design represented as a network of device-independent components, such as primitives, gates and flip-flops, into a network of device-specific components, such as PFUs and EBRs or configurable logic blocks. In this section, you'll analyze different report files and discover cross probing options in each view.



**To run the Map process:**

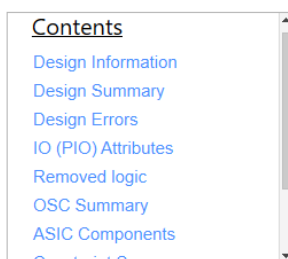
1. From the Process Toolbar, open Task Detail View  and double-click Map Design (or double click on Map design).



When finished, check the icon next to Map Design. A green check mark  indicates success; a red X  indicates failure.


Report files appear in the Reports Browser (If Report Browser is not open click on View > Reports). To view each process report, select the process in the Project Summary pane. Reports include Synthesis Reports, Map Reports, Place & Route Reports, Export Reports, and Misc Reports. Additional reports are available within each category.

2. From Project Summary, choose Map Reports > Map.

The Map Report appears in the right panel as shown in Figure 32, Hover your cursor over Contents (top right corner of the report) to display the MAP Report table of contents.



In Project Summary, if a report has been generated, the icon appears as . If the report has not yet been generated, the icon appears as .

When the report is outdated, the icon appears with a question mark . Use the scroll bar to navigate through the report. Some of the reports are divided into sections.

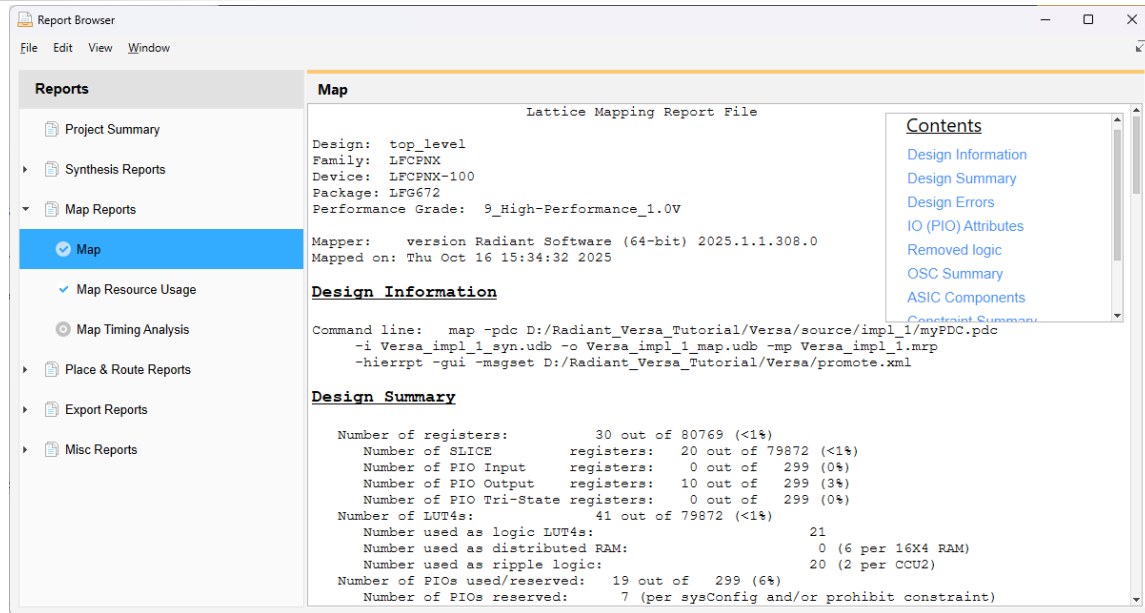


Figure 6 : MAP Report

## Task 8: Running Place and Route

After a design has undergone the necessary translation to bring it into the physical design format during mapping, it is ready for placement and routing. Placement is the process of assigning the device-specific components produced by the mapping process to specific locations on the device floorplan taking into consideration design constraints entered.

After placement is complete, the route phase establishes physical connections between different placed components through available routing options.

### To run place and route:

1. From the Process Toolbar click Place & Route Design.

The place and route tools run. Intermediate results appear in the Output frame of the Lattice Radiant™ main window.




2. From the Report Browser tab, you can directly click on Place & Route Report. Expand the Place & Route Report section. Select Place & Route. Details about Place & Route appear in the right pane of the Reports view.
3. From Place & Route Report, select Place & Route Timing Analysis.

The Place & Route Timing Analysis Report appears in the right pane of the Reports view. All timing constraints and design performance will be listed in this section. We will discuss more about this in later sections.

4. Choose Tools > Physical Designer or click  on the Lattice Radiant™ software toolbar.

The Physical Designer appears.

5. Click Detach Tool icon  at the upper-right corner to detach the tool as shown in Figure 33.

Physical Designer is a combined GUI interface for both the Placement Mode and Routing Mode accessible within this one Lattice Radiant™ software tool. This provides a central location where a user can do all the floor-planning and be able to view the physical layout of the design.

Click on View> Placement Display> Display Connections To/From Selection(s).

Click on View> Placement Display> Display connection outside of selection.

This allows you to see connection to and from the selected object/PFU.

Select one object from the instances listed in the left pane to see similar view to Figure 33.

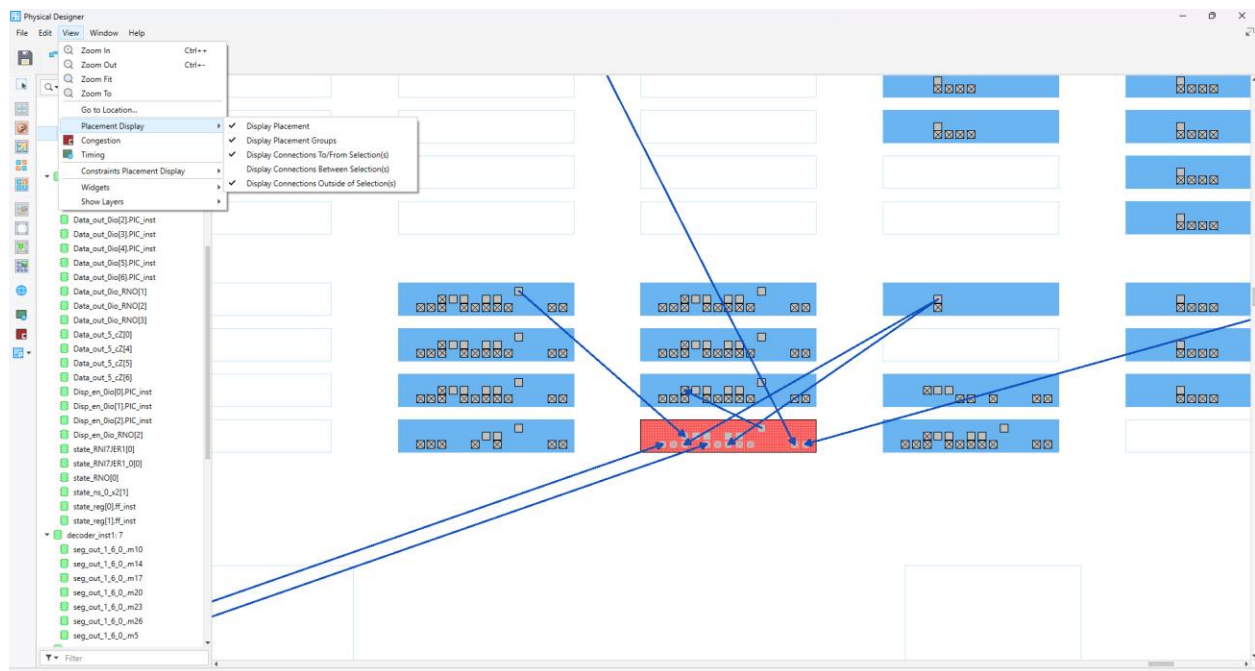






Figure 7: Physical Designer

6. To zoom into a component:

- ▶ Click the name of the component in the list to the left of the diagram.
- ▶ Magnify the surrounding area by clicking and dragging a box around it from left to right.
- ▶ Or click the zoom     buttons.

7. In the diagram, right-click on the component and choose Physical Designer Routing Mode, as shown in Figure 35: Physical Designer Routing View, to display the Floorplan View.

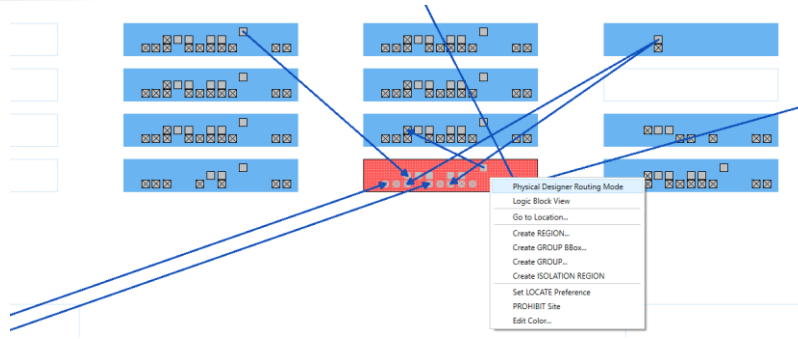


Figure 8: Physical Designer-Cross Probing

Routing Mode provides a detailed read-only layout of your design that includes switch boxes and physical wire connections. Routed connections are displayed as Manhattan-style lines, and unrouted connections are displayed as fly lines. As you move your mouse slowly over the layout, the name and location of each REGION, group, component, port, net, and site are displayed as tool tips.

The routing mode toolbar (View > Show layers) allows you to select the types of elements that will be displayed on the layout.

- **Switchboxes:** display routing switchboxes.
- **Sites:** Displays sites, unused or vacant blocks to which logic can be assigned.
- **Components:** Displays components, blocks that have assigned logic.
- **Routes:** Displays routes, physical connections between resources on the chip after the design has been routed.
- **Ratsnests:** Displays unrouted nets, those that PAR failed to route or those that could not be routed because a site associated with a net was unlocked by the user.
- **Delay Path:** Displays the latest timing path selected in Timing Analyzer.

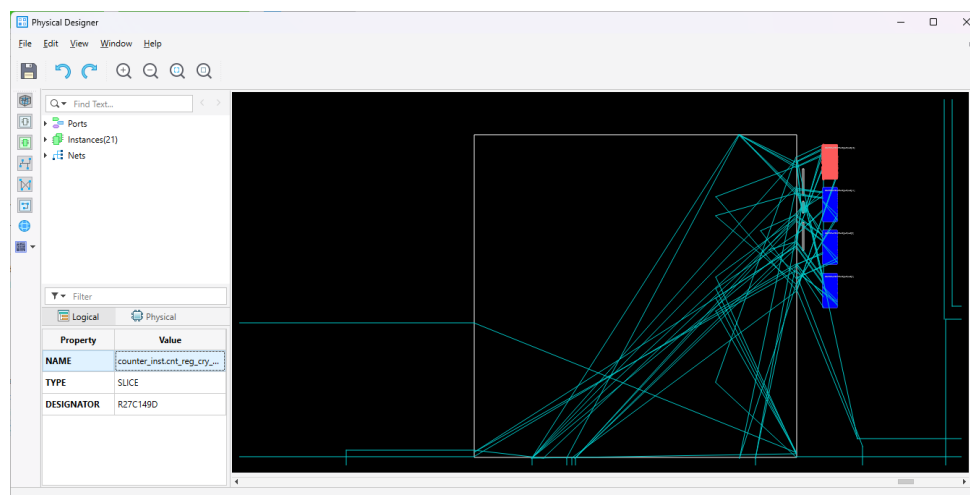
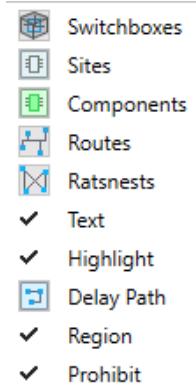


Figure 35: Physical Designer Routing View

8. Close Physical Designer View tab.

## Task 9: Examine Post Place and Route Results

Static timing analysis (STA) can determine if your circuit design meets timing constraints and validates if the design can operate reliably in hardware. STA tool uses user timing constraint and PVT (Process, Voltage, Temperature) device timing characterization to calculate worst case operating scenario and confirm if the design meets setup and hold time requirements.

**To examine timing analysis results:**

9. Choose Tools > Timing Analyzer, or click  on the Lattice Radiant™ software toolbar.

Timing Analysis View appears as shown in Figure 36.

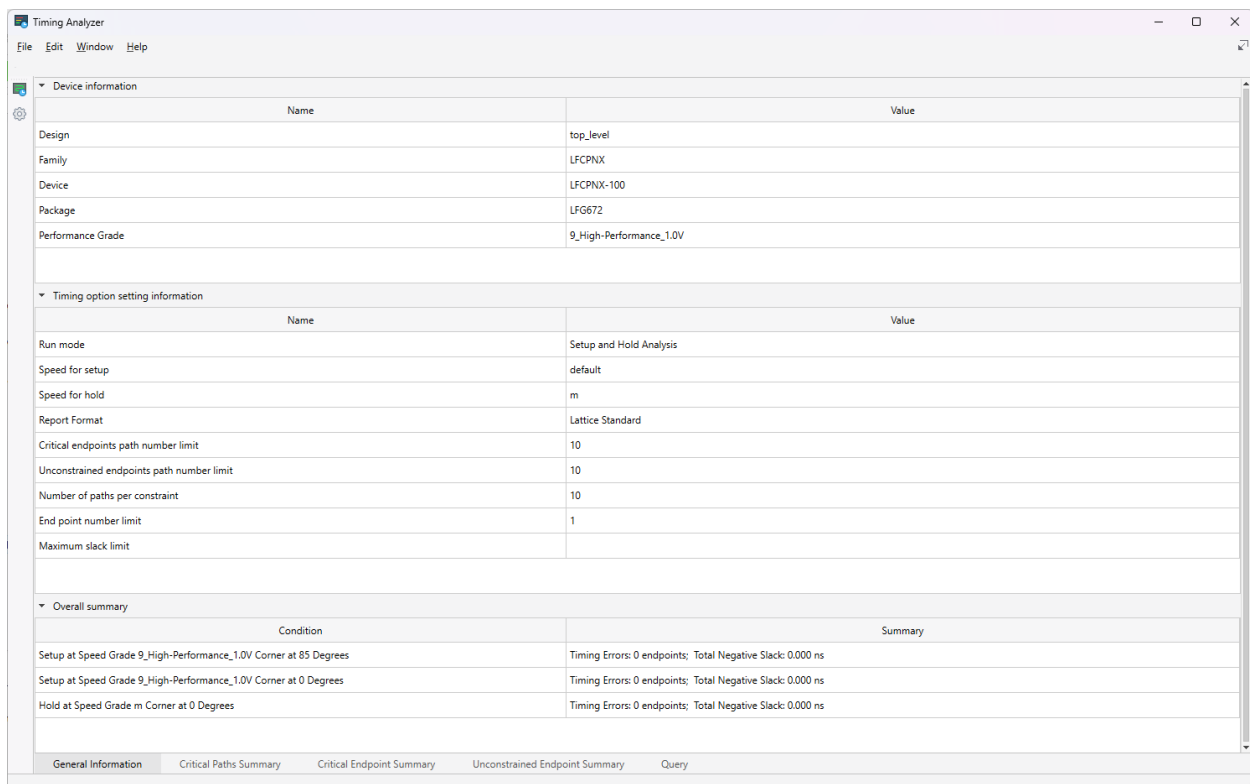


Figure 9: Timing Analyzer View

10. Click the Critical paths summary tab (on the lower-left of the Timing Analysis view) to see top critical paths.

11. Click on Query tab to get details about certain timing paths.

- a. Select one of the output pins of components in the instance list (e.g: counter\_inst/cnt\_reg[12].ff\_inst/Q) and add it to the “From” list as shown below:

- b. Click on **“Search”**
- c. This will display all the timing paths starting from the register output.
- d. Select one of the paths from the search result to get details about Datapath, clock path and waveform view (in different tabs).

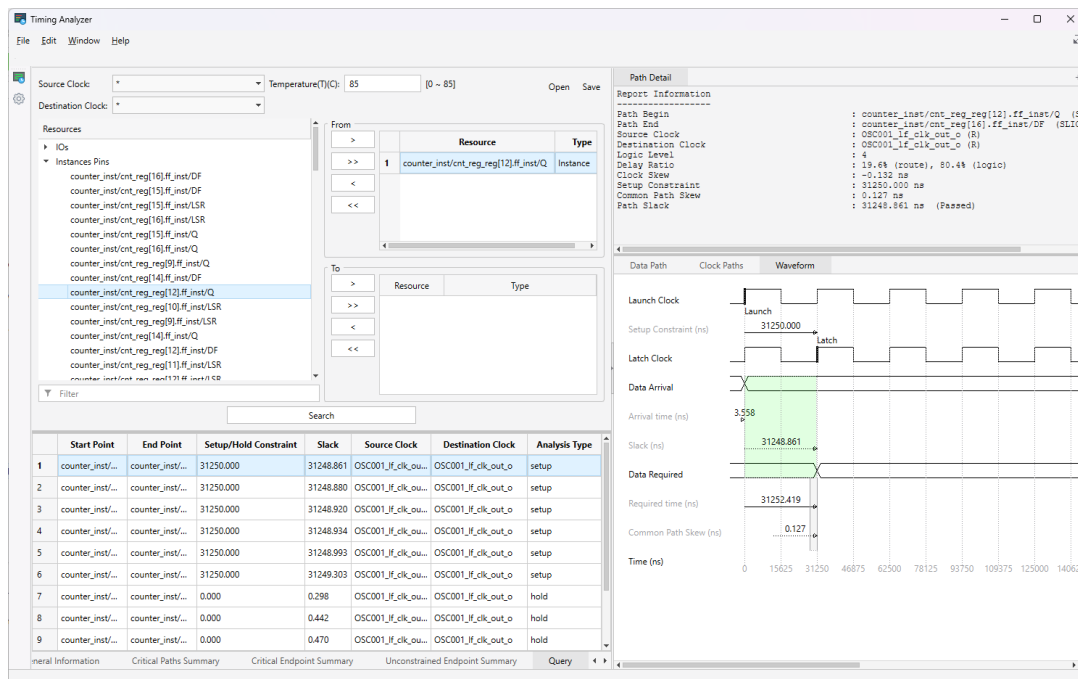


Figure 37: Timing analyzer - Waveform view

## 12. Choose Edit > Timing Option Setting.

The Timing Option Setting dialog box appears, as shown in Figure 38.

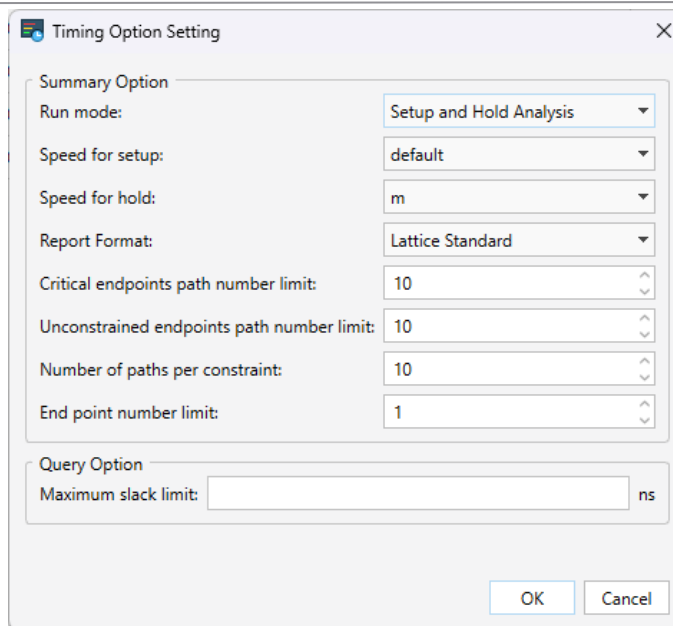


Figure 38: Timing Setting Dialog Box

13. Enter 20 into the “Number of paths per constraint” field to get more critical paths listed (same for paths per constraint or unconstrained paths).
14. Click OK. The Timing Analysis View is refreshed using the new settings.
15. Close the Timing Analysis View.

## Task 10: Analyze Power Consumption

Included with the Lattice Radiant™ software is Power Calculator, which estimates the power dissipation for a given design. Power Calculator uses parameters such as voltage, temperature, process variations, air flow, heat sink, resource utilization, activity, and frequency to calculate the device’s static and dynamic power consumption.

### To analyze power consumption:

10. Choose Tools > Power Calculator or click  on the Lattice Radiant™ software toolbar.

Power Calculator opens in calculation mode.

Power Calculator provides two modes for reporting power consumption:

#### ► Estimation Mode:

In estimation mode, Power Calculator provides estimates of power consumption based on the device resources or template that you provide. This mode enables you to estimate the power consumption for your design before the design is complete or even started.

► **Calculation Mode:**

In calculation mode, Power Calculator calculates power consumption based on device resources taken from a design .udb file, or from an external file such as a value change dump (.vcd) file, after placement and routing. This mode is intended for accurate calculation of power consumption, because it is based on the actual device utilization.

Editing data in white cells, such as voltage, frequency, activity factor, and thermal data, does not change mode. Editing data in yellow cells, such as design data, will change calculation mode to estimation mode.

1. Click Detach Tool icon  at the upper-right corner to detach Power Calculator from the Lattice Radiant™ software main window, as shown in Figure 39.

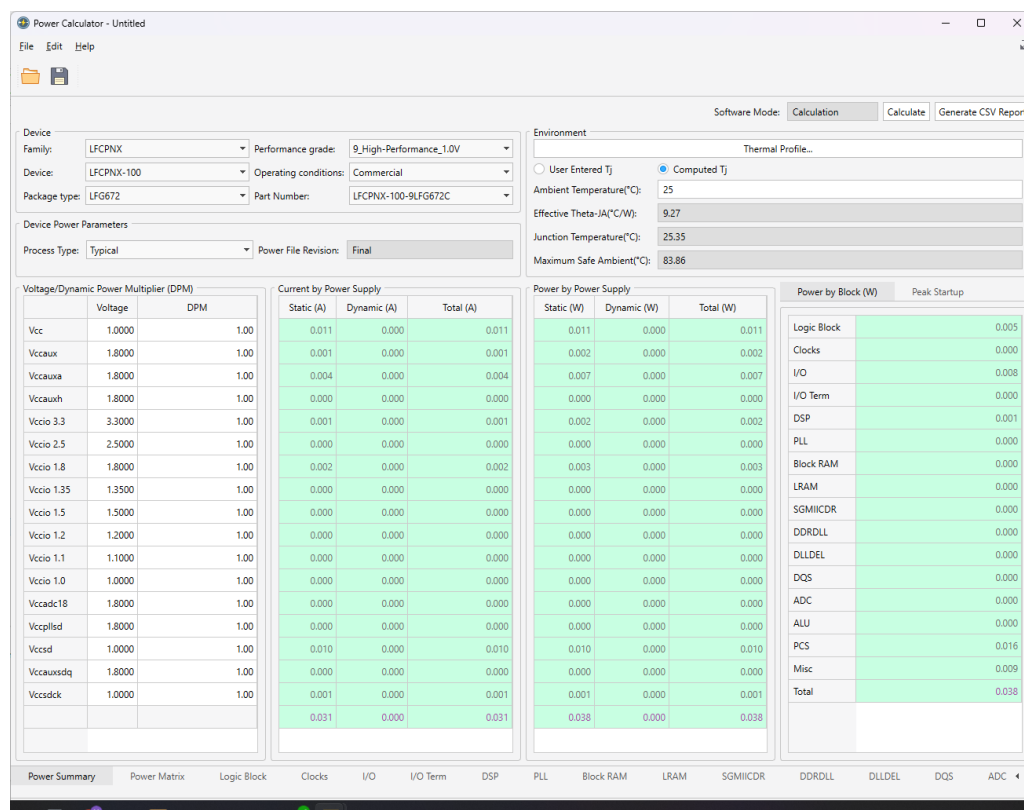


Figure 10: Power Calculator

2. In the Device Power Parameters section select the following parameters:

Process Type: **Worst.**

3. Click the Thermal Profile button in the Environment section.

The Power Calculator – Thermal Profile dialog box appears.

4. In the Board Selection section, choose the following parameter: Small board.



5. Click **OK**.
6. Click on **Calculate**.



You should see power numbers and temperature results updated based on the new settings.

In the title bar of Power Calculator, "Untitled" appears with an asterisk, which indicates an in-memory change to the timing constraints. You can save the change to a Power Calculator File (.pcf) by choosing File > Save File As and giving it a name and location. The .pcf file will then appear in the Analysis Files folder of the File List Pane.

7. Close Power Calculator. If you chose not to save in the previous step, a Save dialog box will now appear. Click No to discard the change.

## Task 11: Run Export Utility Programs

Use the Process Toolbar to generate files for exporting. One of the exported files will be a bitstream file (.bin) which will be used to program Lattice CertusPro-NX™ device in the next steps.

11. Click the Task Detail View  to see detailed information on the processes.
12. With Export Files, you have more options that you can select (No need to select these):
  - a. IBIS Mode
  - b. Gate-Level Simulation File
13. Click the Run button  on the Process Toolbar.

The Lattice Radiant™ software generates the selected files and saves them in your project directory.



## Task 12: Download a Bitstream to an FPGA

This task requires you to have a Lattice CertusPro-NX™ Versa Board. In the previous section, you generated export files including a bitstream file (.bin). In this section, you will use the Lattice Radiant™ software Programmer to download a bitstream to CertusPro-NX FPGA mounted on a Versa board.

This tutorial design allows you to display counter direction and count on a 7-Segment display on the versa board. For reference, the architecture of the design includes the following blocks as shown in Figure 40:

- MyOSC block: Generate a low frequency clock to drive the logic in the design
- Counter: an 18-bit counter with direction control (UP or DWN)
- Seven Segment decoder: used to decode the count value into the 7-segment for display
- Counter\_fsm: There are 3 x 7-segment displays that are driven by the same bus with enable signals for each. The FSM selects which 7-display to enable based on the data on the bus.

The following block diagram shows how the different design components are connected (Synthesis output).

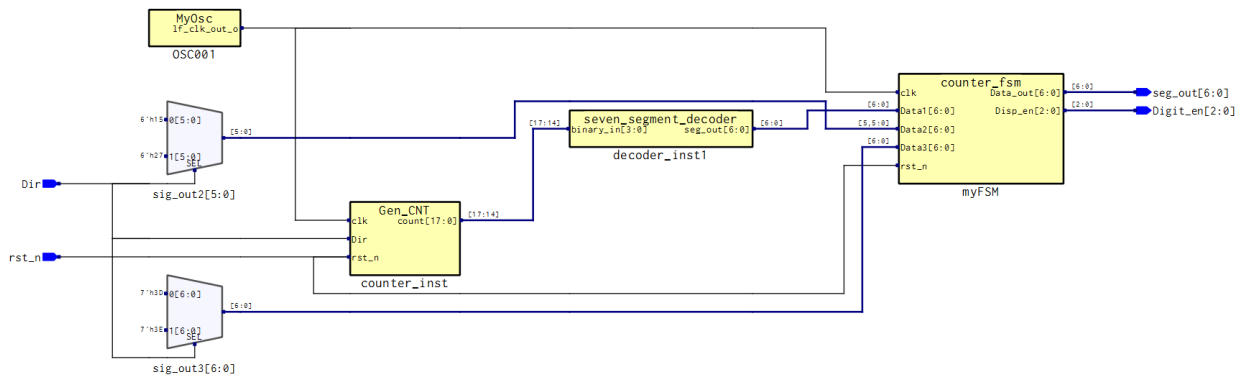


Figure 11: Design block Diagram

This table describes the ports and signals of the design.

Table 1: Ports and Signals		
Port type	name	Description
Input Ports	Rst_n	Active low reset signal connected to SW3 on the board
	Dir	Select the counter direction. Connected to the pin 1 of SW1 on the board
Output Ports	Seg_out	7 bit 7-Segment Display data bus connected to the 3 displays
	Disp_En	3-bit Enable signal connected to the 3 displays

You can refer to the Lattice CertusPro-NX™ versa board user guide for further details on the board. Figure 41 shows the location of certain switches and components on the board.

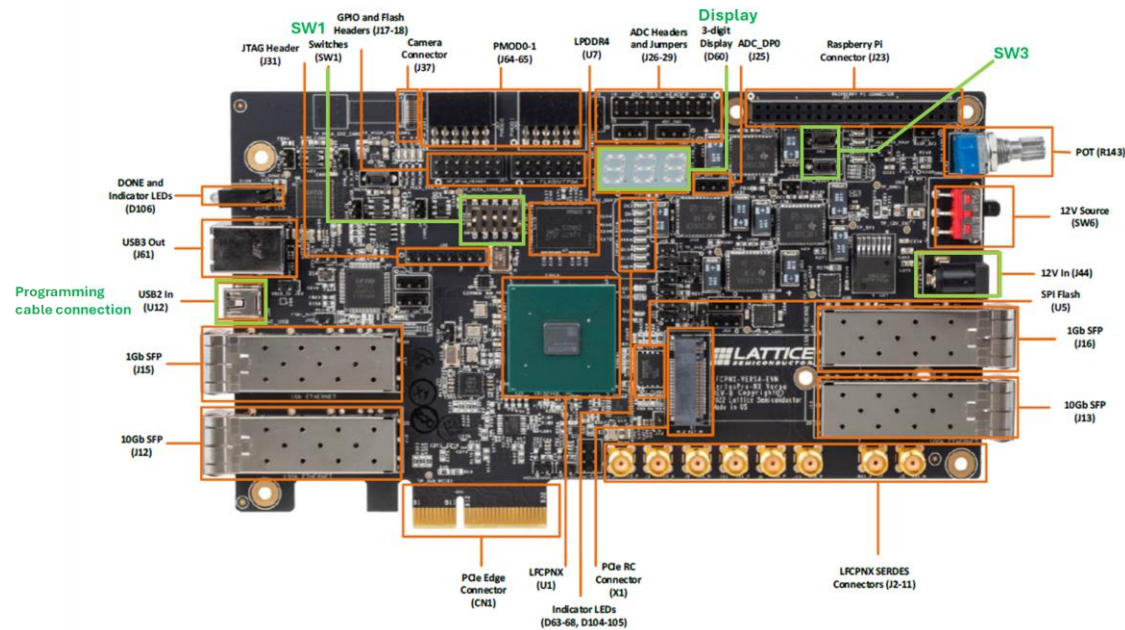



Figure 41: Lattice CertusPro-NX™ Versa board main components

### To download the bitstream to the FPGA on the board:

1. Connect a USB cable from your computer to the Versa Board. Give the computer a few seconds to detect the USB cable.
2. Choose Tools > Programmer or click  on the Lattice Radiant™ software toolbar. The Programmer opens, automatically detects the USB cable, and scans the board. You should see similar interface to Figure 42

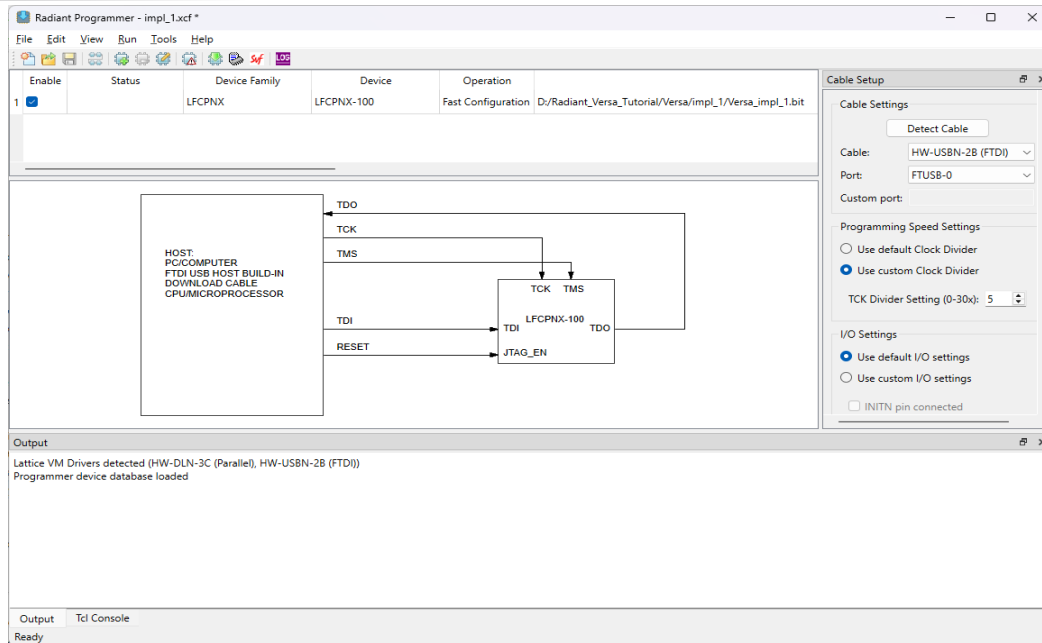


Figure 12-Programmer interface

3. Optional Step: in case of an issue, you can perform the following to detect the cable:
  - a. In the Cable Setup box, click Detect Cable.
  - b. Cable should be set at HW-USB-2B (FTDI).
  - c. Port should be set to FTUSB-0.
4. Optional Step: Ensure that the proper device is selected by doing the following:
  1. Click in the Device Family column and choose LFCPNX from the pull-down menu.
  - b. Click in the Device column and choose LFCPNX-100 from the pull-down menu.
5. Right-click on any cell and choose Device Properties to open the Device Properties dialog box.
6. Ensure the settings are as follows:
  - ▶ For Target Memory, choose Static Random Access Memory (SRAM) from the pull-down menu.
  - ▶ For Port Interface, choose JTAG from the pull-down menu.
  - ▶ For Access Mode, choose Direct Programming from the pull-down menu.
  - ▶ For Operation, choose Fast Configuration from the pull-down menu.
  - ▶ For the programming file, browse to <Project Directory>/impl\_1/Versa\_impl1.bin, as shown in Figure 43.

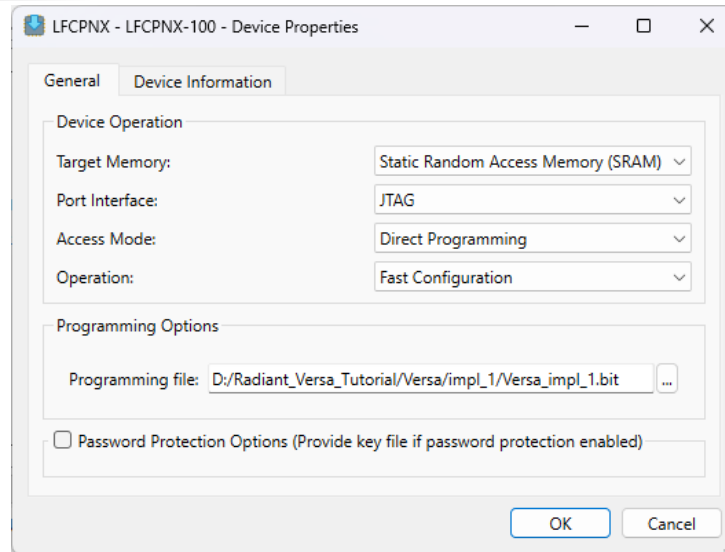



Figure 43: Device Properties Dialog Box

7. Click **OK**.
8. In Programmer, choose Run > Program Device or click  on the Programmer toolbar to initiate the download.
6. If the programming process succeeds, you will see a green-shaded PASS in Programmer's Status column. Check the Programmer output console to see if the download passed.

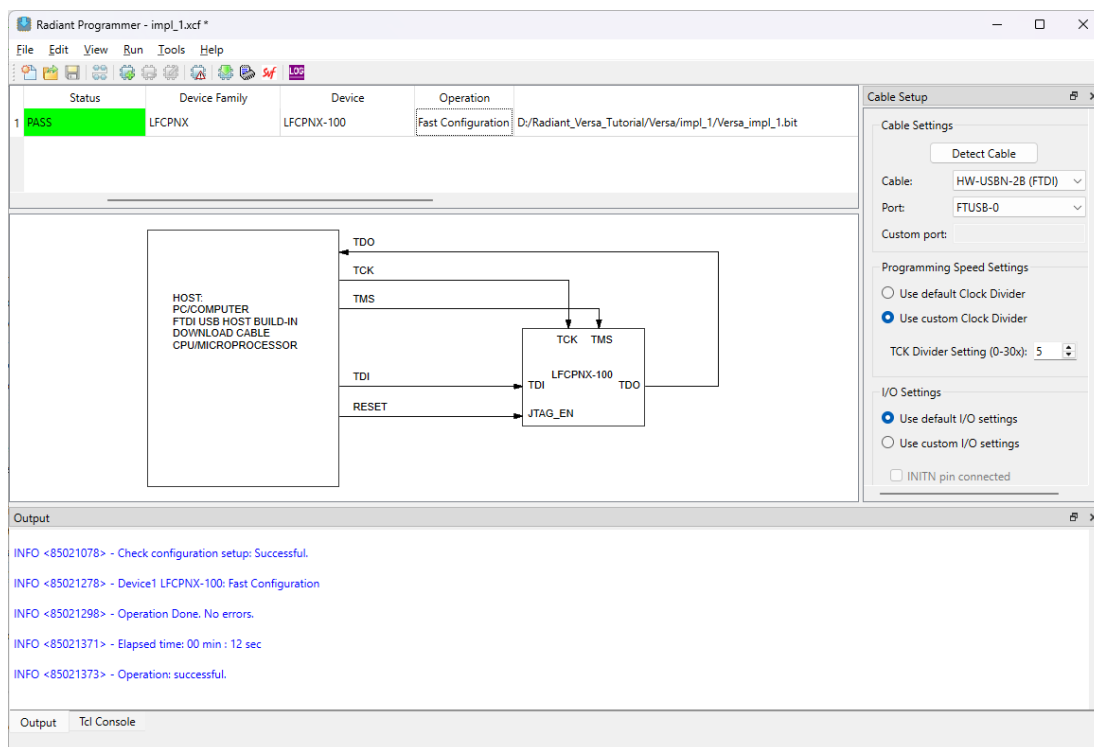


Figure 44: Lattice Programmer – Successful Programming

At this point you should see the 7-Segment display Counting UP or DN with incremental values. You can change counter direction by flipping bit 1 of SW1 switch (if you are using the remote lab, this may not be an option).




Figure 45: Evaluation Board - programmed

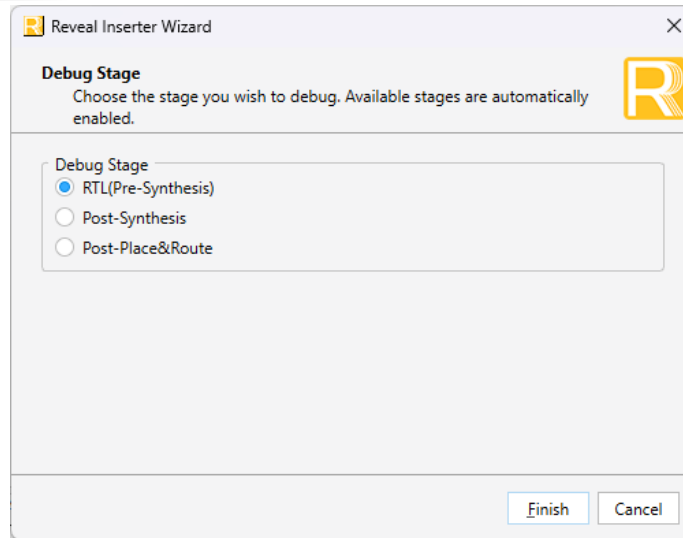
## Task 13: Use Reveal Inserter to Add On-Chip Debug Logic

In this task, you will use Reveal Inserter to configure a Reveal core based on triggering conditions and the desired trace buffer. The primary output of Reveal Inserter is a modified version of your design with one or more cores instantiated and the core logic ready for mapping, placement, and routing.


**To generate and add a Reveal core:**

### Setting Up the Logic Analyzer trace signals

1. Choose Tools > Reveal Inserter or click  on the Lattice Radiant™ software toolbar. Radiant supports Reveal inserter at different implementation stages (RTL, Post synthesis or Post Place & Route). For this tutorial we will use RTL debug stage as shown below:



2. Figure 46: Reveal Wizard - Debug Stage

3. Click **Finish**.
4. Click Detach Tool icon  at the upper-right corner to detach Reveal Inserter.
5. Click Add core and select Add Logic Analyzer. You should see an interface like below with all signals in your design on the left and Logic analyzer setting on the right.

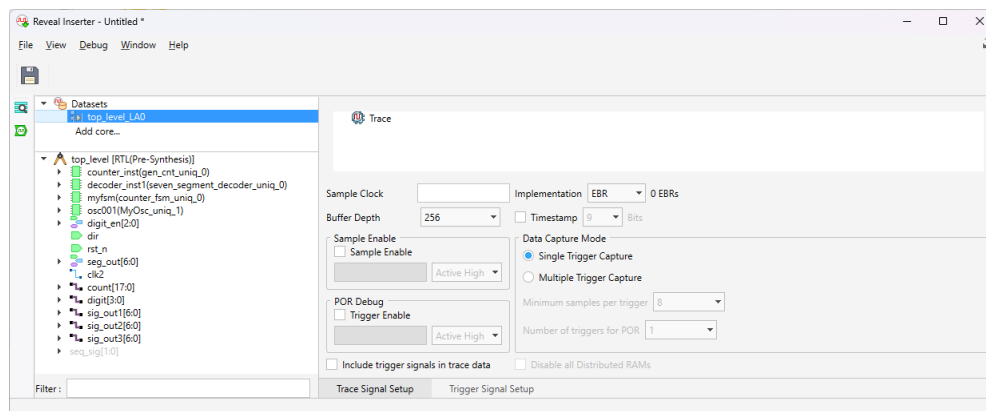


Figure 47: Reveal Inserter Main Window

6. Click on the Trace Signal Setup tab, if it is not already selected.
7. From the Design Tree tab, expand the top module.
8. Drag the following signals from the Design Tree pane to the Trace Data pane.
  - ▶ Digit\_en,
  - ▶ Seg\_out,

- ▶ Myfsm/state,
  - ▶ Decoder\_inst1/seg\_out
  - ▶ Decoder\_inst1/binary\_in
9. Select the Include trigger signals in trace data option.
  10. Drag the **clk1** signal from the Design Tree pane to the Sample Clock box
  11. From the pull-down menu in the Buffer Depth box, select 256.

## Setting Up the Trigger Units

In this section, you will set up under what condition the Logic analyzer should trigger.

### To set up the trigger units:

1. Click on the Trigger Signal Setup tab.
2. Click Add to add a trigger unit condition.
3. Drag the **dir** signal from the Design Tree pane to the Signals (MSB:LSB) box in row 1 of the Trigger Unit pane.
4. Click Add to add a second trigger unit.
5. Drag the **Myfsm/state** signal from the Design Tree pane to the Signals (MSB:LSB) box in row 2 of the Trigger Unit pane.
6. Add a third line with Decoder\_inst1/binary\_in
7. Leave all other values as default.

## Setting Up the Trigger Expressions

Now you will set up the trigger expressions in the Trigger Expression section of the tab.

### To set up the trigger expressions:

1. Click Add in the Trigger Expression window. In the Name box in the Trigger Expressions section, use the default name of TE1.
2. In the Expression box, type TU1 and then Enter on your keyboard. The RAM Type automatically changes to 3 Slices.
3. Click on add to add another trigger expression
4. In the Expression box, type TU2 and then Enter on your keyboard. The RAM Type automatically changes to 3 Slices.



- Click on add to add another trigger expression
- In the Expression box, type TU3 and then Enter on your keyboard. The RAM Type automatically changes to 3 Slices.
- The Trigger Signal Setup tab should now resemble Figure 48. You have the option to change the value associated with Trigger Units (e.g. State == DISP1)

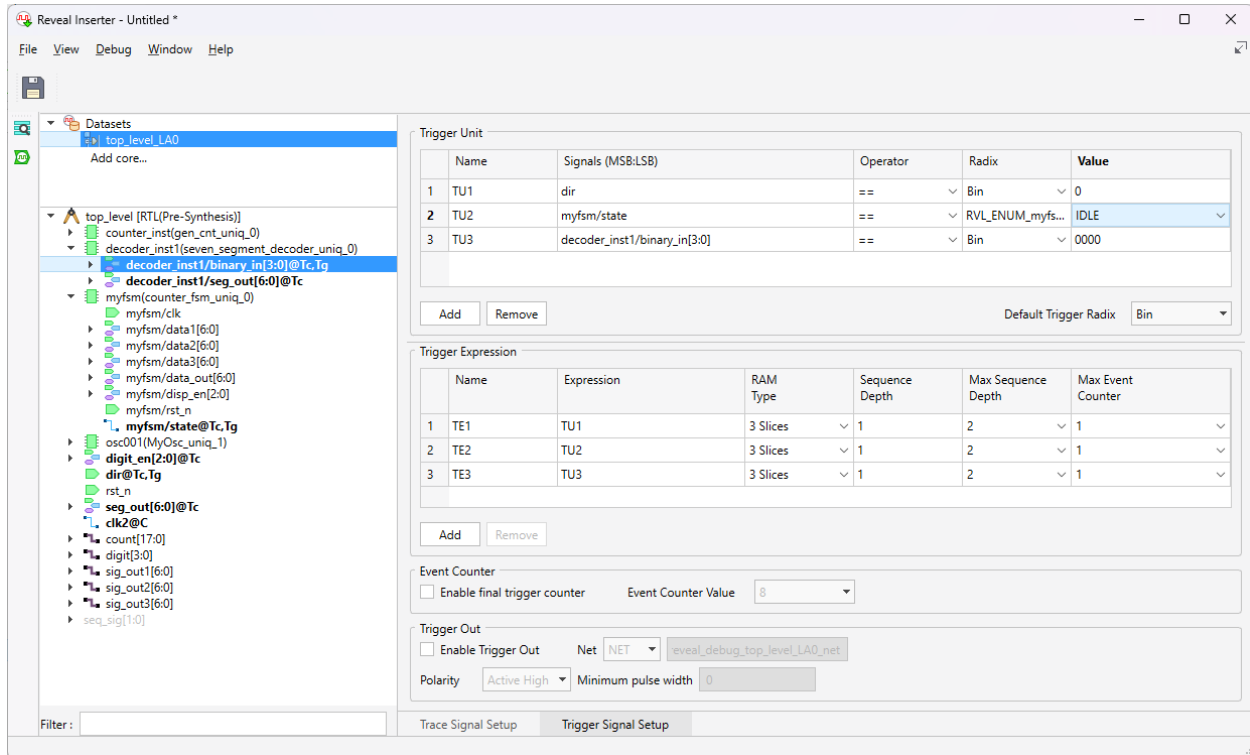



Figure 48: Reveal Trigger Signal Setup Tap

## Inserting the Debug Logic

Now you will insert the debug logic into the design project.

### To insert the debug logic:

- Choose Debug > Insert Debug or click .
- In the Insert Debug to Design dialog box, shown in Figure 49, be sure that the Activate Reveal File in Design Project option is selected.

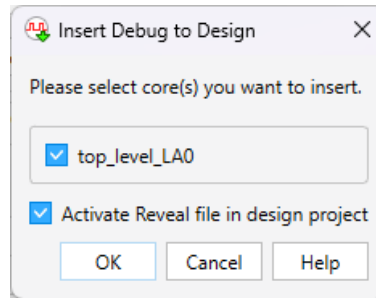


Figure 49: Reval Insert Debug to Design Dialog Box

3. Click OK. The Save Reveal Project dialog box opens.
4. Name the file **Versa\_LA**.
5. Click Save. The .rvl file is added to the Debug Files folder in the File List view, as shown in Figure 50.

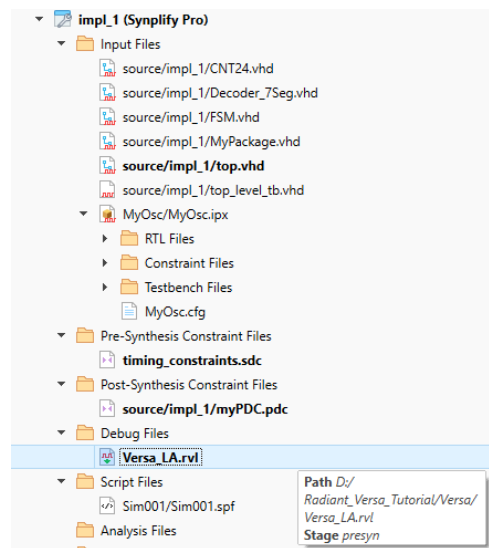


Figure 50: File List with Reveal Debug File

8. **Close** Reveal Inserter.



## Generating a Bitstream and Programming the FPGA

Use the Process Toolbar to generate a bitstream (export files) and use Programmer to download the bitstream to the FPGA. This task assumes that the Board is connected to your computer with a download cable.

### To generate a bitstream:

1. Click the Run button  on the Lattice Radiant™ software Process Toolbar.

The Lattice Radiant™ software generates the selected files and saves them in your project directory.

2. If Programmer is not already open, choose Tools > Programmer, or click  on the Lattice Radiant™ software toolbar.
3. Ensure that the bitstream file named Versa\_impl\_1 is selected as the programming file (check modified date to make sure you are using the latest version generated).
4. Click **OK**.
5. In Programmer, choose Run > Program Device or click  on the Programmer toolbar to initiate the download.
6. If the programming process succeeded, you will see a green-shaded PASS in the Programmer Status column. Check the Programmer output console to see if the download passed.
7. Close Programmer.

A dialog box opens asking if you want to save your changes.

8. Click **No**.

## Task 14: Use Reveal Logic Analyzer to Perform Logic Analysis


In this task, you will use Reveal Logic Analyzer to set up trigger conditions and view trace buffer data from the on-chip Reveal core operating within the target.

The trigger setup determines the specific conditions and how the Reveal core trace signal status is displayed in Reveal Logic Analyzer's graphical user interface. You will explore just a few ways to trigger and trace the system.

### Creating a New Reveal Logic Analyzer Project

You must first create a Reveal Analyzer project.

#### To create a new Reveal Logic Analyzer project:

1. In the Lattice Radiant™ software main window, choose Tools > Reveal Analyzer/Controller or click  on the Radiant software toolbar.

The Reveal Analyzer Startup Wizard dialog box appears, as shown in Figure 51.

2. In the upper left of the dialog box, select Create a new file.
3. Type Versa\_Analyzer in the box to name the file.

The Reveal analyzer will be stored in .rva extension automatically.

4. In the pull-down menu on the top row next to the file name, Click Detect.

The cables connected to the PC are listed in the USB Port box. Choose Lattice HW-USBN-2B (FTDI) from the drop-down menu if not already selected automatically.

5. In the RVL Source box, browse to <project\_directory>/Versa\_LA.rvl (make sure you are using the latest version created, in case there are multiple .rvl files created)
6. Click Scan to detect the hardware connected to the cable

### Note

Reveal uses a signature authentication mechanism to verify that the instantiated core and the hardware match. Having the wrong reveal in hardware or software will generate an error.

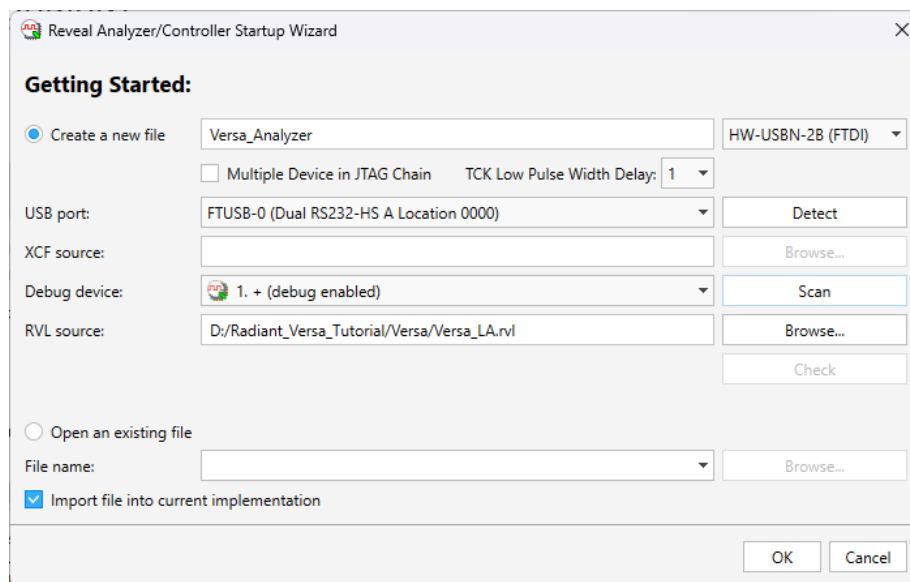



Figure 51: Reveal Analyzer Startup Wizard

7. Click OK. Reveal Logic Analyzer appears
8. Click Detach Tool icon  at the upper-right corner to detach the tool.

The Reveal Logic Analyzer window now appears with the LA Trigger tab selected, as shown in Figure 52. It contains the same trigger units and trigger expressions that you set up in Reveal Inserter.

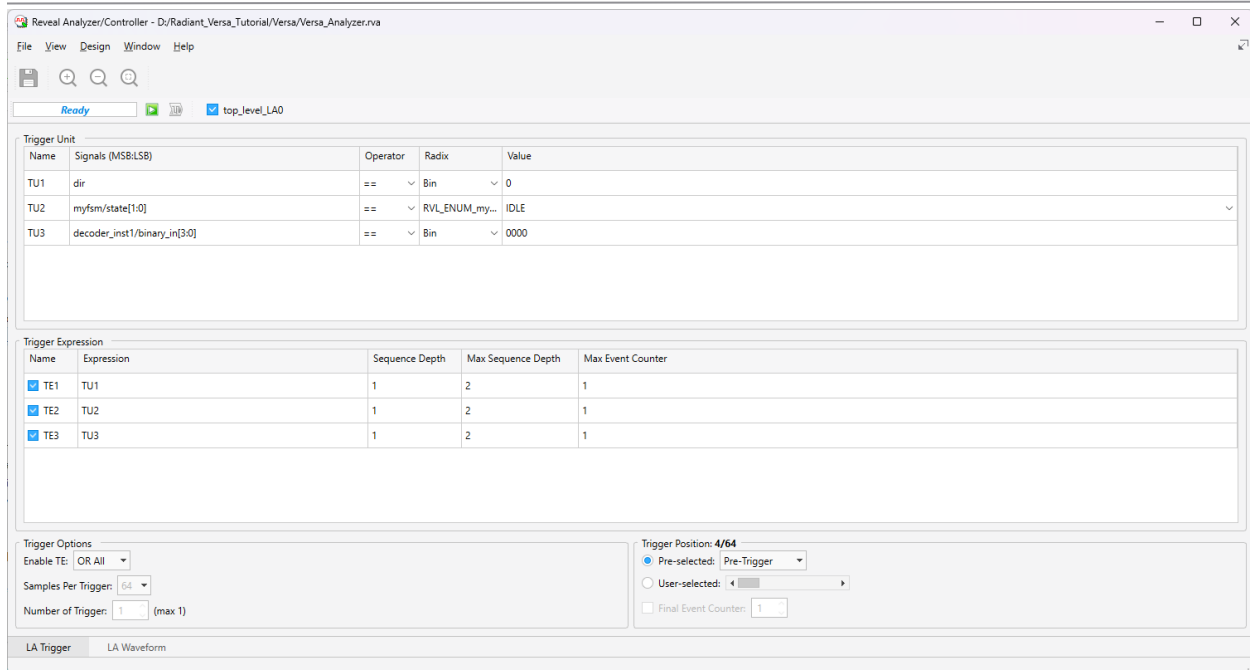


Figure 52: Reveal Analyzer Trigger settings

## 9. The default Trigger Position is: Pre-selected: Pre-Trigger. Change it to center trigger.

In the Trigger position section, you can specify the trigger position relative to the trace data. The numbers in the section title show the current position. The two options to choose from include:


- ▶ Pre-selected allows you to choose one of the standard positions.
  - ▶ Pre-Trigger: 16/256 of the way from the beginning of the samples.
  - ▶ Center-Trigger: 128/256 of the way from the beginning of the samples.
  - ▶ Post-Trigger: 240/256 of the way from the beginning of the samples.
- ▶ User-selected allows you to choose a position with the slider.


Follow Figure 52 or choose your own parameter for the different settings.

## Running Logic Analyzer

Now that Reveal Logic Analyzer is set up, you can run Logic Analyzer.

### To capture data:

1. Click on the LA Waveform tab.
2. Click the Run  button in the Reveal Analyzer toolbar.

The Run button changes into the Stop  button and the status bar next to the button shows the progress (Connecting, Running, Completed).

Reveal Analyzer first configures the modules selected for the correct trigger condition, then waits for the trigger conditions to occur. When a trigger occurs, the data is uploaded to your computer. The resulting waveforms appear in the LA Waveform tab.

- You have the option to do manual trigger If no trigger occurs by clicking on Manual Trigger  button.

You should now see the waveforms displayed as shown in Figure 53.



Figure 13: Reveal Analyzer waveforms

- Close Reveal Analyzer. A dialog box opens asking if you want to save your changes.
- Click **No**.
- To close the design project, choose File > Close Project. The Save Modified Files dialog box opens.
- To save the files, click OK. To discard the changes, click Deselect All and then click **OK**.

The design project and associated tools are close. The Lattice Radiant™ window returns to the Start Page.

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## Summary of Accomplishments

You have completed the Lattice Radiant™ Software Tutorial for Lattice CertusPro-NX™. In this tutorial, you have learned how to:

- ▶ Create a new Lattice Radiant™ software project.
- ▶ Create a new module using IP Catalog.
- ▶ Verify functionality with simulation.
- ▶ Inspect strategy settings.
- ▶ Examine resources.
- ▶ Set timing and location assignments.
- ▶ Run synthesis process.
- ▶ Run map design and check reports.
- ▶ Run place and route.
- ▶ Examine post place and route results.
- ▶ Analyze power consumption.
- ▶ Run Export Utility programs (Generate bitstream).
- ▶ Download a bitstream to an FPGA.
- ▶ Use Reveal Inserter to add on-chip debug logic.
- ▶ Use Reveal Logic Analyzer to perform logic analysis.

## Recommended References

You can find additional information on the subjects covered by this tutorial in the Lattice Radiant™ software online Help, and in the Lattice Radiant Software User Guide.